μPD7220A
High-Performance
Graphics Display Controller

Description

The μPD7220A high-performance graphics display controller (HGDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the HGDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the HGDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the HGDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the HGDC is ideal for advanced computer graphics applications.

For a more detailed description of the HGDC's operation, please refer to the 7220/7220A design manuals.

System Considerations

The HGDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the HGDC's design, each of the system components is used to the maximum extent through a six-level hierarchy of simultaneous tasks. At the lowest level, the HGDC generates the basic video raster timing, including sync and blanking signals. Partitioning areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the HGDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the HGDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the HGDC takes care of the high-speed and repetitive tasks required to implement a graphics system.

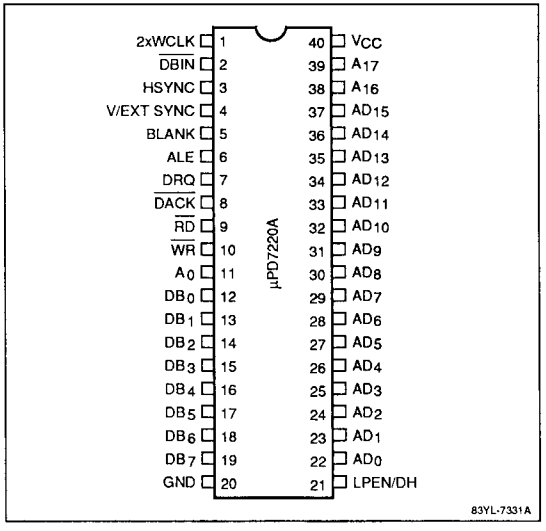
Features

- ☐ Microprocessor interface
  - — DMA transfers with 8257- or 8237-type controllers
  - — FIFO command buffering
- ☐ Display memory interface
  - — Up to 256K words of 16-bits
  - — Read-modify-write (RMW) display memory cycles as fast as 500 ns
  - — Dynamic RAM refresh cycles for nonaccessed memory
- ☐ Light pen input
- ☐ Drawing hold input
- ☐ External video synchronization mode
- ☐ Graphic mode
  - — Four megabit, bit-mapped display memory
- ☐ Character mode
  - — 8K character code and attributes display memory
- ☐ Mixed graphics and character mode
  - — 64K if all characters
  - — 1 megapixel if all graphics
- ☐ Graphics capabilities
  - — Figure drawing of lines, arc/circles, rectangles, and graphics characters in 500 ns per pixel
  - — Display 1024-by-1024 pixels with 4 planes of color or grayscale
  - — Two independently scrollable areas
- ☐ Character capabilities
  - — Auto cursor advanced
  - — Four independently scrollable areas
  - — Programmable cursor height
  - — Characters per row: up to 256
  - — Character rows per screen: up to 100
- ☐ Video display format
  - — Zoom magnification factors of 1 to 16
  - — Panning
  - — Command-settable video raster parameters
- ☐ NMOS technology
- ☐ Single +5 V power supply
- ☐ DMA capability
  - — Bytes or word transfers
  - — 4 clock periods per byte transferred
- ☐ On-chip pull-up resistor for VSYNC/EXT, HSYNC and DACK, and a pull-down resistor for LPEN/DH

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7220AD	40-pin ceramic DIP	6 MHz
μPD7220AD-1	40-pin ceramic DIP	7 MHz
μPD7220AD-2	40-pin ceramic DIP	8 MHz

Pin Configuration



Character Mode Pin Utilization

Pin No.	Pin Symbol	Function
35-37	AD_{13}-AD_{15}	Line counter bits 0 to 2 outputs
38	AD_{16}	Line counter bit 3 output
39	AD_{17}	Cursor output and line counter bit 4

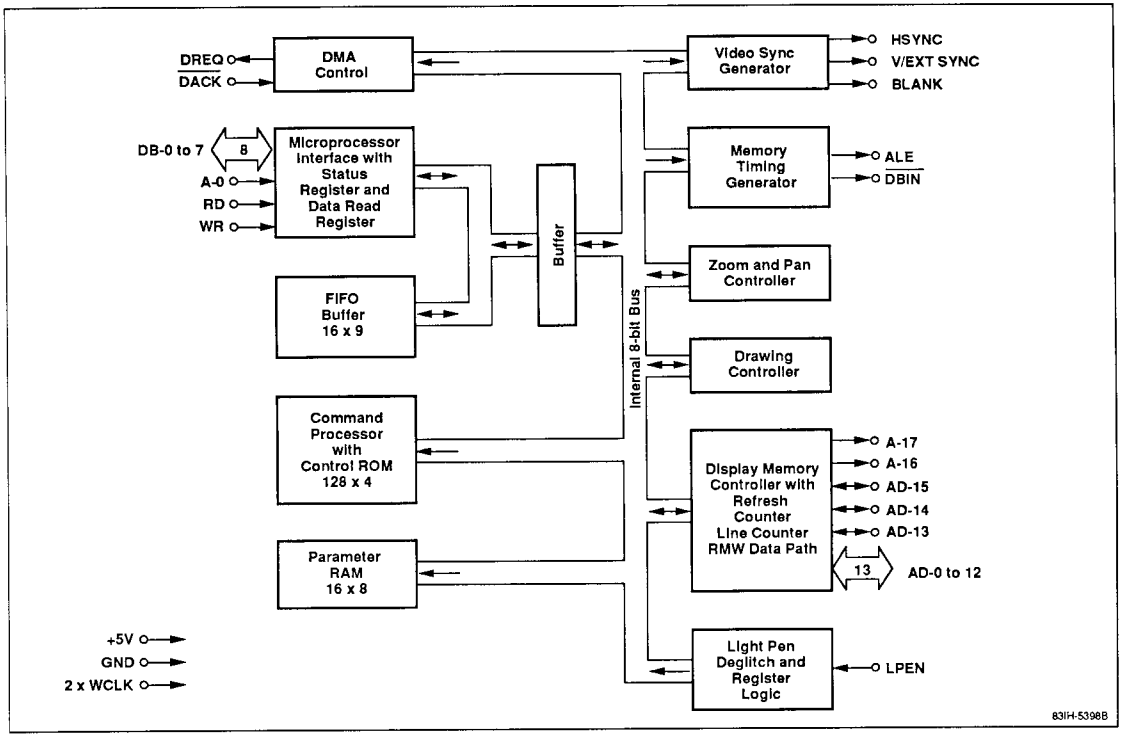
Mixed Mode Pin Utilization

Pin No.	Pin Symbol	Function
35-37	AD_{13}-AD_{15}	Address and data bits 13 to 15
38	A_{16}	Attribute blink and clear line counter output
39	A_{17}	Cursor and bit-map area flag output

Pin Identification

Pin No.	Pin Symbol	Function
1	2xWCLK	Clock input
2	DBIN	Display memory read input flag
3	HSYNC	Horizontal video sync output
4	V/EXT SYNC	Vertical video sync output or external VSYNC input
5	BLANK	CRT blanking output
6	ALE	Address latch enable output
7	DRQ	DMA request output
8	DACK	DMA acknowledge input
9	RD	Read strobe input for microprocessor interface
10	WR	Write stobe input for microprocessor interface
11	A_0	Address select input for microprocessor interface
12-19	DB_0-DB_7	Bidirectional data bus to host microprocessor
20	GND	Ground
21	LPEN/DH	Light pen detect input drawing hold input
22-34	AD_0-AD_{12}	Address data lines to display memory
35-37	AD_{13}-AD_{15}	Utilization varies with mode of operation
38	A_{16}	Utilization varies with mode of operation
39	A_{17}	Utilization varies with mode of operation
40	V_{CC}	+5 V ±10% power supply

Block Diagram



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