FEATURES

- **1MByte Frame-Buffer on a single chip**
- **1.6 G-Bytes/Second Internal Bus:**
  - **Fast Window Drawing Operations**
  - **Fill at up to 1.6 GByte/Second**
  - **Aligned BitBLT at up to 0.64 G-Bytes/Second**
- **8-Column Block Write with Bit and Byte Masking Capability**
- **200 MBytes/Second CPU Read / Write Data Path :**
  - **Fast Image Read / Writes**
  - **20ns Ultra Fast Page Mode (t_{UPC}) with EDO**
- **4 Each $\overline{BE}$ and $\overline{OE}$ for Byte-Write / Read Control**
- **Dual 128 Byte Split Serial Register**
  - **Dual Buffers Relax System Timing**
  - **71.4MHz Serial Clock Frequency**
- **5.0V ± 10% Supply Voltage**
- **TTL I/O Level Compatible**
- **120-Pin PQFP**

KEY TIMING PARAMETERS

Parameter \ Speed	-60	-70	-80
RAM read/write & block ultra fast page cycle time (t_{UPC})	20ns	25ns	30ns
$\overline{RAS}$ access time (t_{RAC})	60ns	70ns	80ns
$\overline{CAS}$ access time (t_{CAC})	12ns	15ns	15ns
$\overline{RAS}$ cycle time (t_{RC})	110ns	130ns	150ns
SAM cycle time (t_{SCC})	14ns	17ns	22ns
SAM access time (t_{SCA})	13ns	15ns	20ns
$\overline{SE}$ access time (t_{SEA})	10ns	12ns	15ns
IDD1 : RAM op. current	160mA	150mA	140mA
IDD2 : Stand-by current	10mA	10mA	10mA
IDD1A : RAM & SAM op. current	190mA	180mA	170mA
IDD2A : SAM op. current	50mA	45mA	40mA

PERFORMANCE

Graphic Operations	Cycle	Peak Performance
10-Pixel Vector	UFW	4.0M Vectors/Sec
7 x 9 Character Draw	UFW	1.7M Characters/sec
FILL	UFBW8	1.6G Bytes/Sec
BitBLT (Vertical Scroll)	UFBR/ UFBWL	0.49G Bytes/Sec

DESCRIPTION

The KM4232W259 is a 1MByte Dual Ported DRAM array with added features that accelerate graphic operations in a GUI environment. A 256-bit internal bus allows transferring up to 32 bytes of data on a single chip. All necessary features present to support fully functional SCROLL and ALIGNED BLOCK-MOVE graphic operations.
The 16-bit Serial Output port is comprised of two 128-byte serial registers. This allows relexed system timing and full CPU access while the registers are being emptied to the display.

To enhance the block transfer performance for Windows-based operations, the KM4232W259 also provides Block Write Mode of 8-columns which allows 32-bytes maximum of block data transfer at a time. A choice of 2-colors can be used in any combination of foreground and background mixing. (e.g., For monochrome and color text expansion) This operation is useful for graphic Fill and Text operations.
A combination of Mixed Modes (see truth table) defined by the $\overline{CAS}$ falling edge is also supported. This performance enhancement feature allows system designers to change the mode of operation on the fly within Ultra Fast Page cycle time.

PIN NAMES

Pin Name	Pin Function
SC	Serial Clock
$\overline{SE}$	Serial Enable
SQ_0–SQ_{15}	Serial Data Output
$\overline{BE}_{0-3}$	Byte Enable
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DSF 0, 1, 2	Special Function Pins
W_0/DQ_0 ~ W_{31}/DQ_{31}	Data Write Mask / Input-Output
A_0 ~ A_8	Address Inputs
NC	(No Connection)
V_{CC}	Power
V_{SS}	Ground

PIN CONFIGURATION

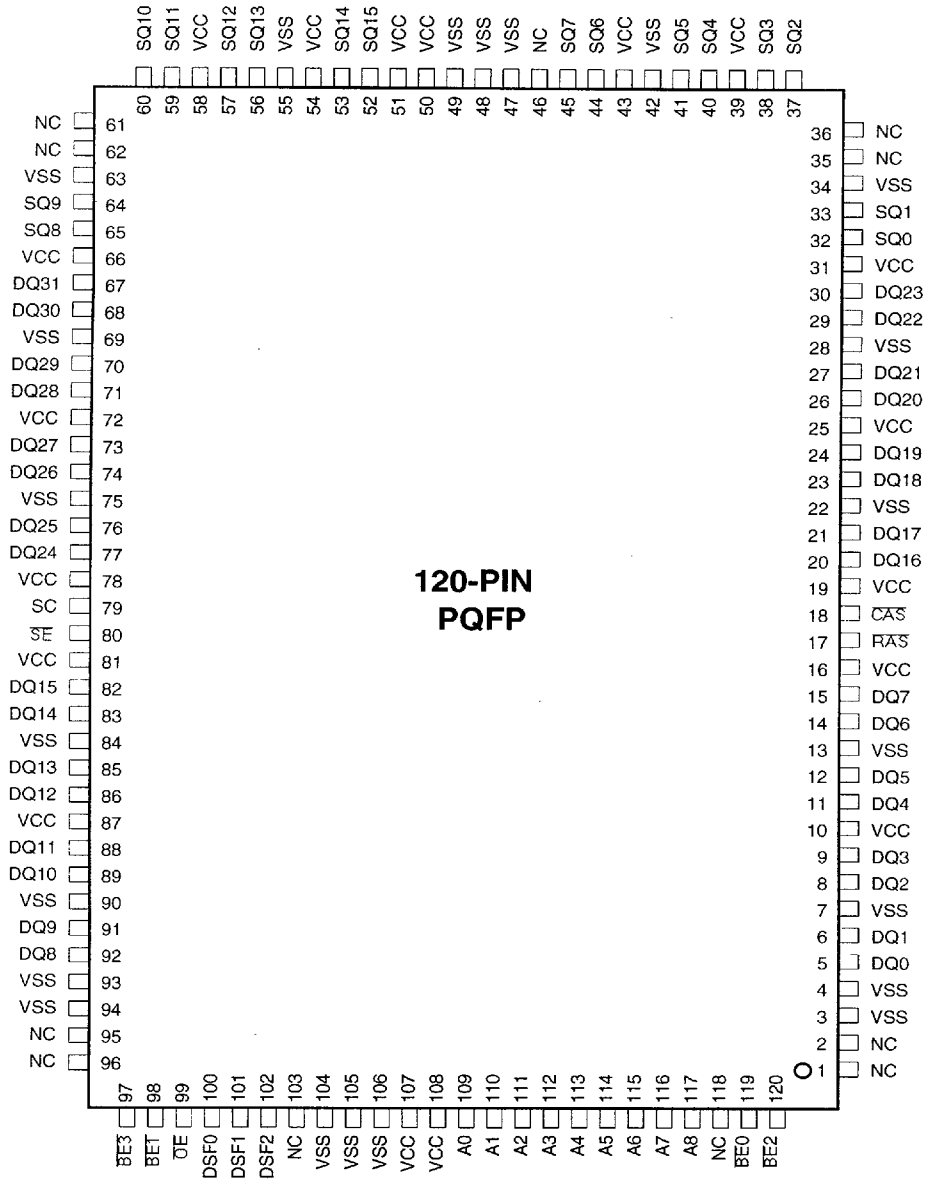


Figure 1. PIN CONFIGURATION

PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTION
SC	INPUT	**Serial Clock** : Clock input to the serial address counter for the SAM registers. The serial access is initiated from SC rising edge. Output data is held until the next clock rising edge.
$\overline{SE}$	INPUT	**Serial Port Enable** : $\overline{SE}$ enables the serial output buffers.
SQ_0 - SQ_{15}	OUTPUT	**Serial Output** : Output pins of the 128 x 16 Serial data register.
$\overline{BE}_{0-3}$	INPUT	**Byte Enable** : These signals enable the random output buffer during read operation or the write driver during write operation. They are latched on the falling edge of $\overline{CAS}$. $\overline{BE}_0$ controls W_0/DQ_0 - W_7/DQ_7.
$\overline{OE}$	INPUT	**Output Enable** : Enables the random output buffer when dropped LOW after $\overline{CAS}$ goes Low. Otherwise the output is in a High-Z state. On the falling edge of $\overline{RAS}$, $\overline{OE}$=HIGH indicates new mask data will be used for the operation. If $\overline{OE}$=LOW, previously loaded mask data is used.
$\overline{RAS}$	INPUT	**Row Address Strobe** : It acts as a master chip enable clock, also serves as a clock to latch the row address (A_0-A_8). It also latches the mask data for bit plane mask when $\overline{OE}$ is HIGH at $\overline{RAS}$ falling edge. $\overline{CAS}$ before $\overline{RAS}$ refresh mode is available if falling edge of $\overline{RAS}$ is preceded by $\overline{CAS}$ =LOW.
$\overline{CAS}$	INPUT	**Column Address Strobe** : Used as a clock, which latches the column address (A_0-A_8) and determines the functionality of mixed mode by monitoring DSF status. It can also initiate the read (EDO *1) or write access to the selected words and transfer the selected data (256 bits) to the SAM register.
DSF0, 1, 2	INPUT	**Special Function Select** : The DSF0, 1, 2 data latched by CAS falling edge is used to indicate which special functions, Block Write, Internal Move, LCR, LMR, Split Read Transfer, Ultra fast page mode read (EDO) and write cycles, are going to be performed.
W_0/DQ_0 - W_{31}/DQ_{31}	INPUT OUTPUT	**Input and Output pin to the RAM** : These pins carry read, write or mask data, depending upon the type of cycle. Refer to $\overline{RAS}$ and $\overline{CAS}$ control cycles truth tables.
A_0 - A_8	INPUT	**Address Input** : The KM4232W259 utilizes a multiplexed addressing method for selecting one word among 256K words of memory cells, 9 row addresses and 9 column addresses are latched by the $\overline{RAS}$ and $\overline{CAS}$ falling edges. Some address pins can be used as control signals in particular cycles (e.g., A_0 for LMR cycle, A_0, A_1 for LCR, UFBW8,SRT/SRTR cycles, and A_0 and A_1 can address the latches during UFBR, UFBWL cycles).

*1 EDO : Extended Data Out

FUNCTIONAL DESCRIPTION

The window RAM (WRAM™) can be divided into four major functional blocks (refer to block diagram). The DRAM array organized as 32 (512 x 512) bit planes, the Serial access memory (SAM), the Read/Write control blocks, and the color registers and data latches block. The WRAM™ cycles can be divided into two major categories, External Data transfer cycles and internal Data transfer cycles.

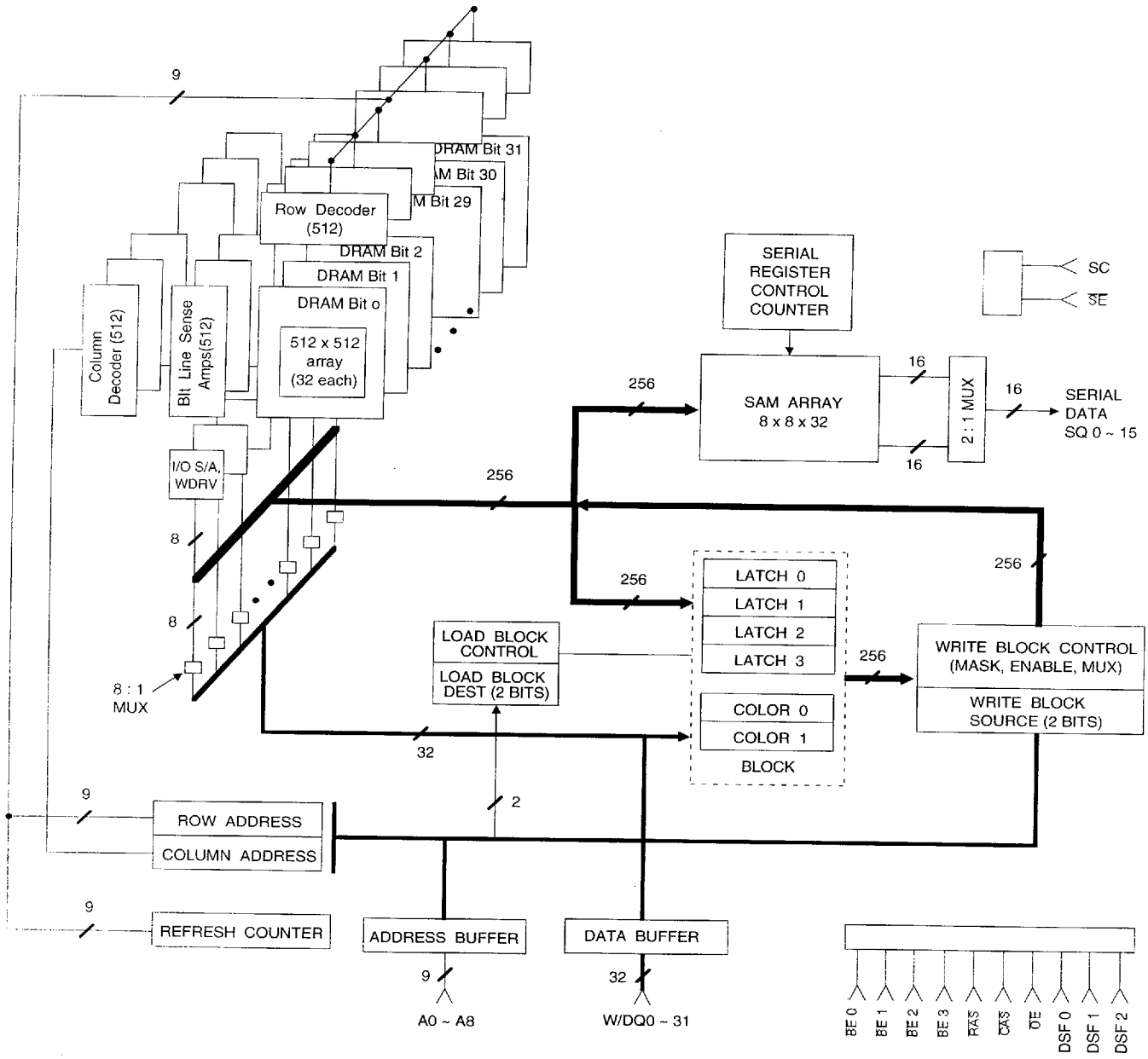


Figure 2. BLOCK DIAGRAM

$\overline{RAS}$ CONTROL CYCLES TRUTH TABLE

$\overline{CAS}$ #2	$\overline{RAS}$ #1							Mnemonic Code	Function
$\overline{BE}_{3-0}$	$\overline{CAS}$	$\overline{OE}$	DSF2	DSF1	DSF0	RA_{8-0}	W_{31-0}		
X	0	X	X	X	0	X	X	RST	Reset Cycle
X	0	X	X	X	1	X	X	CBR	CBR Refresh
⇧ (Note 2)	1	0/1 (Note 1)	X	X	0	ROW	WPB Mask	RW/ ROR	New ROW initiation for any RW cycle, RAS only Refresh
X	1	0/1 (Note 1)	X	X	1	X	WPB Mask		Vendor Specific mode

Notes :

1. $\overline{OE}$ = 1 updates MASK Register content. $\overline{OE}$ = 0 uses previously loaded Mask data.
2. ⇧ = Byte Control (refer to Byte Enable Truth Table).

BYTE ENABLE TRUTH TABLE

$\overline{CAS}$ #2		OPERATION
$\overline{BE}_0$	O	Byte Read/Write Enable (DQ_0-DQ_7)
	1	Byte Read/Write Disable (DQ_0-DQ_7)
$\overline{BE}_1$	O	Byte Read/Write Enable (DQ_8-DQ_{15})
	1	Byte Read/Write Disable (DQ_8-DQ_{15})
$\overline{BE}_2$	O	Byte Read/Write Enable (DQ_{16}-DQ_{23})
	1	Byte Read/Write Disable (DQ_{16}-DQ_{23})
$\overline{BE}_3$	O	Byte Read/Write Enable (DQ_{24}-DQ_{31})
	1	Byte Read/Write Disable (DQ_{24}-DQ_{31})

RESET Cycle

	AFTER RESET CYCLE
Color Register 0, 1	Reset to "0"
Mask Register	Reset to "1" : non-masking mode
SAM Transfer Counter	Reset to "0" : Address the first Row of SAM (first SAM)

$\overline{CAS}$ CONTROL CYCLES TRUTH TABLE

$\overline{CAS}$ #2														
$\overline{BE}_{3-0}$ (Note 2)	DSF2	DSF1	DSF0	CA 8	7	6	5	4	3	2	1	0	W_{31}/DQ_{31}- W_0/DQ_0	Mnemonic Code	Function
X	1	0	1	X	X	X	X	X	X	X	0/1	0	Pixel Color Data	LCR	Load Color Reg 0 or 1 (Note 5)
X	1	0	1	X	X	X	X	X	X	X	X	1	Mask Data(WPB)	LMR	Load Mask Reg (Note 1)
X	0	0	0	←Column Address→						X	0	0	X X X X	UFBR	DRAM to Latch 0
				←Column Address→						X	0	1	X X X X		DRAM to Latch 1
				←Column Address→						X	1	0	X X X X		DRAM to Latch 2
				←Column Address→						X	1	1	X X X X		DRAM to Latch 3
⇧	0	1	1	←Column Address→						X	0	0		UFBWL (Note 3)	Latch 0 to DRAM
				←Column Address→						X	0	1			Latch 1 to DRAM
				←Column Address→						X	1	0	←Byte Mask→		Latch 2 to DRAM
				←Column Address→						X	1	1			Latch 3 to DRAM
⇧	0	0	1	←Column Address→						X	0	0	←Byte Mask→	UFBW8 (Note 3)	From Color Reg 0 to DRAM
				←Column Address→						X	0	1	←Byte Mask→		From Color Reg 1 to DRAM
				←Column Address→						X	1	0	←Col Reg Select→	(Note 4)	C0(Di=0), C1(Di=1) to DRAM
				←Column Address→						X	1	1	←Col Reg Select→		C0(Di=1), C1(Di=0) to DRAM
X	0	1	0	←Column Address→						X	0	0	X X X X	SRT	Split Read Transfer
X	0	1	0	←Column Address→						X	0	1	X X X X	SRTR	Split Read Transfer with SAM Pointer Reset
⇧	1	1	0	←Column Address→									D_{OUT} (31~0)	UFR	Ultra Fast Page Read Cycle
⇧	1	1	1	←Column Address→									D_{IN} (31~0)	UFW	Ultra Fast Page Write Cycle

Notes :

1. LMR cycle always updates Mask Register content. Wi=1 enables write to Bit plane i, Wi=0 disables (maskes) write to Bit plane i
2. =Byte Control (refer to Byte Enable Truth Table)
3. Wi (i = 0, ..., 31) performs Byte Masking during UFBWL and UFBW8 cycles.
   ⇧Wi = 1 enables Byte write to Byte i.
   Wi = 0 disables (Masks) Byte Write to Byte i.
4. Di (i = 0, ..., 31) Selects either color Register 0 (C_0) or Color Register 1 (C_1) to be written into DRAM.
5. CA1=0 accesses color Register 0, CA1=1 accesses color Register 1.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to VSS	V_{IN}, V_{OUT}	-1.0 to +7.0	V
Voltage on VCC Supply Relative to VSS	VCC	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1.2	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS (Voltage reference to Vss, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ground	VSS	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	6.5	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter (RAM Port)	SAM Port	Symbol	Speed			Unit
			-60	-70	-80	
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling at t_{RC} = min)	Standby	I_{DD1}	160	150	140	mA
	Active	I_{DD1A}	190	180	170	mA
Standby Current ($\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}) DSF 0 ~ 2 = V_{IL}	Standby	I_{DD2}	10	10	10	mA
	Active	I_{DD2A}	50	45	40	mA
$\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling at t_{RC} = min)	Standby	I_{DD3}	160	150	140	mA
	Active	I_{DD3A}	190	180	170	mA
$\overline{CAS}$ -Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling at t_{RC} = min)	Standby	I_{DD4}	160	150	140	mA
	Active	I_{DD4A}	190	180	170	mA
Ultra Fast Page Mode Current (LCR, LMR, RCR, RMR, UFR and UFW Cycles)* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling at t_{UPC} = min)	Standby	I_{DD5}	190	170	150	mA
	Active	I_{DD5A}	210	190	170	mA
Ultra Fast Page Mode Current * (UFBWL and UFBW8 Cycles) ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling at t_{UPC} = min)	Standby	I_{DD6}	220	200	180	mA
	Active	I_{DD6A}	240	220	200	mA
Ultra Fast Page Mode Current * (UFBR, SRT and SRTR Cycles) ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling at t_{UPC} = min)	Standby	I_{DD7}	220	200	180	mA
	Active	I_{DD7A}	240	220	200	mA

* Real values are dependent on output loading and cycle rates. Specified values are obtained with the output open ($\overline{SE}$=$\overline{OE}$=V_{IH}). I_{DD} is specified average current ; In I_{DD1}, I_{DD3}, address transition once while $\overline{RAS}$ = V_{IL}.
In the I_{DD5}, I_{DD6}, I_{DD7} address transition should be changed only once while $\overline{CAS}$ = V_{IH}.
SAM standby condition ; $\overline{SE}$ ≥ V_{IH}, SC ≤ V_{IL} or ≥ V_{IH}.

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Rating	Rating	Unit
Input Leakage Current (Any Input ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts).	I_{IL}	-10	10	μA
Output leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 6.5V)	I_{OL}	-10	10	μA
Output High Voltage Level (RAM I_{OH} = -2mA, SAM I_{OH} = -2mA	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL} = 2mA, SAM I_{OL} = 2mA)	V_{OL}	-	0.4	V

CAPACITANCE (V_{CC} = 5V, f=1MHz, T_A=25°C)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	3	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{BE}_{0-3}$, $\overline{OE}$, $\overline{SE}$, SC, DSF_{0-2})	C_{IN2}	3	6	pF
Input/Output Capacitance (W_0/DQ_0-W_{31}/DQ_{31})	C_{DQ}	3	7	pF
Output Capacitance (SQ_{0-15})	C_{SQ}	3	7	pF

AC OPERATING CONDITIONS (Voltage reference to Vss, T_A = 0 to 70°C)

Parameter	Unit
AC input levels	V_{IH}/V_{IL} = 3.0V/0.0V
Output measurement reference level	1.4V
Input rise and fall time	tr/tf = 2ns/2ns

AC CHARACTERISTICS (0 °C TA 70°C, VCC = 5V ±10%, see Notes 1 and 2)

Parameter	Symbol	-60ns		-70ns		-80ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{CAS}$	tCAC		12		15		15	ns	3,5,6
Access time from $\overline{CAS}$ precharge	tCPA		25		32		39	ns	3
Access time from column address	tAA		25		30		35	ns	3,8
Access time from output enable	tOEA		12		15		15	ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,5,8
Access time from SC	tSCA		13		15		20	ns	4
Access time from $\overline{SE}$	tSEA		10		12		15	ns	4
$\overline{BE}$ hold referenced to $\overline{CAS}$	tCBH	0		0		0		ns	
$\overline{BE}$ setup referenced to $\overline{CAS}$	tBSC	8		9		12		ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ hold time (CBR refresh)	tCHR	10		12		15		ns	
$\overline{CAS}$ precharge time (Ultra Fast Page Mode)	tCP	8		9		12		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	9	10K	12	10K	ns	
$\overline{CAS}$ setup time (CBR refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ to output in Low-Z	tCLZ	5		5		5		ns	3,9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
$\overline{CAS}$ to SC setup (SRT cycle)	tCSS	6 SC	112 SC	6 SC	112 SC	6 SC	112 SC	CLK Rising	13
$\overline{CAS}$ to SC setup (SRTR and first SRT cycle)	tSRTR	18		22		25		ns	10
Column address hold time	tCAH	0		0		0		ns	
Column address setup time	tASC	8		9		12		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Data hold time	tDH	0		0		0		ns	
Data setup time	tDS	8		9		12		ns	
Data to $\overline{CAS}$ delay	tDZC	0		0		0		ns	
$\overline{OE}$ high hold time from $\overline{CAS}$ Low	tOH	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	tCFH	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$	tRFH	8		10		15		ns	
DSF setup referenced to $\overline{CAS}$	tFSC	8		9		12		ns	
DSF setup referenced to $\overline{RAS}$	tFSR	0		0		0		ns	
Output enable to data input delay	tOED	7		8		9		ns	
Output buffer Turn-off delay from $\overline{CAS}$ ($\overline{RAS}$=High)	tOFF	3	7	3	8	3	9	ns	7

AC CHARACTERISTICS (continued)

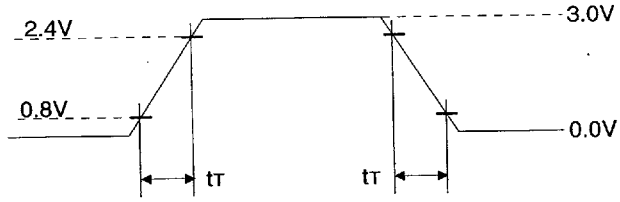
Parameter	Symbol	-60ns		-70ns		-80ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn-off delay from $\overline{OE}$	tOEZ	3	7	3	8	3	9	ns	7
$\overline{OE}$ high to $\overline{CAS}$ low setup time	tOSC	17		19		23		ns	
$\overline{OE}$ hold referenced to $\overline{RAS}$	tORH	8		10		15		ns	
$\overline{OE}$ setup referenced to $\overline{RAS}$	tORS	0		0		0		ns	
RAM output hold time from $\overline{CAS}$	tCOH	3		3		3		ns	
Random read or write cycle time	tRC	110		130		150		ns	
$\overline{RAS}$ hold time	tRSH	15		20		25		ns	
$\overline{RAS}$ prechagre time	tRP	40		50		60		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	10		10		10		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width (Ultra Fast Page Mode)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	25	45	30	50	35	60	ns	5
$\overline{RAS}$ to column address delay time	tRAD	15	35	20	40	25	50	ns	8
$\overline{OE}$ to $\overline{CAS}$ high setup time to see valid output	tOCS	5		5		5		ns	
$\overline{CAS}$ high to $\overline{OE}$ low delay time to hide the output	tCOD	5		5		5		ns	
Output buffer turnoff delay from $\overline{CAS}$ when $\overline{BE}$ is high at falling edge of $\overline{CAS}$	tBEZ	3	7	3	8	3	9	ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
Read-Write cycle time	tPCRW	35		43		47		ns	
Refresh period (512 cycle)	tREF		17		17		17	ms	
Row address hold time	tRAH	8		10		15		ns	
Row address setup time	tASR	0		0		0		ns	
SC cycle time	tSCC	14		17		22		ns	
SC hold referenced to $\overline{CAS}$ (SRTR and first SRT cycle)	tCSTR		4		4		4	ns	10
SC precharge (SC low time)	tSCP	5		6		7		ns	
SC Pulse width (SC high time)	tSC	5		6		7		ns	
Serial out buffer turn-off from $\overline{SE}$	tSEZ	3	6	3	7	3	8	ns	7
Serial output hold time from SC	tSOH	3		3		3		ns	
Transition time (rise and fall)	tT	2	30	2	30	2	30	ns	2,11
Ultra Fast Page mode cycle time	tUPC	20		25		30		ns	

AC CHARACTERISTICS (continued)

Parameter	Symbol	-60ns		-70ns		-80ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write per bit mask data hold	tMH	8		10		15		ns	
Write per bit mask data setup	tMS	0		0		0		ns	
$\overline{CAS}$ precharge time for entering CBR test cycle	tCPT	40		45		50		ns	
$\overline{RAS}$ pulse width for CBR test cycle	tRAST	80	100K	90	100K	100	100K	ns	
Serial output buffer turn-on from $\overline{SE}$	tSEO	5		5		5		ns	4,9
Output buffer turn-on delay from $\overline{OE}$	tOEO	5		5		5		ns	3,9
$\overline{RAS}$ to SC delay (SRTR cycle and first SRT cycle)	tRSD	60		70		80		ns	10
SE Precharge time	tSEP	5		6		7		ns	

Notes :

1. An intial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 SC cycles before proper device operation is achieved ($\overline{OE}$ & $\overline{SE}$ = HIGH). If the internal refresh counter is used, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles. A Reset cycle must be executed right after the 8 initialization cycles to ensure proper device operation.
   A Reset cycle should be excuted only right after power-up. It should never be excuted during operation because this would bring the WRAM back to the initial state right after power-up.
2. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max), and are assumed to be 2ns for all inputs.
3. RAM port outputs are measured with a load equivalent to 1 TTL loads and 50pF. DOUT comparator level : VOH/VOL=1.4V
4. SAM port outputs are measured with a load equivalent to 1 TTL loads and 30pF. DOUT comparator level : VOH/VOL=1.4V
5. Operation within the tRCD(max) limit insures the tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
6. Assumes that tRCD ≥ tRCD(max).
7. The parameters tOFF, tOEZ, and tSEZ define the time at which the output achieves the open circuit condition. tOFF is determined by the rising edge of $\overline{RAS}$ or $\overline{CAS}$ whichever comes later.
8. Operation within the tRAD(max) limit insures that tRCD(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
9. The parameters tSEO and tCLZ define the time at which the output achieves low-Z state.
10. tCSTR, tSRTR, tRSD only apply to the SRTR cycle and the very first SRT cycle after power up (i.e., the very first SRT cycle after power up is equivalent to a SRTR cycle).
11. Operating input condition.



Input signals transition levels are from 0.0V to 3.0V for AC testing.
All timing levels are referenced from VIL(max) and VIH(min) with transition time of 2.0ns

12. Power Recommended be applied to the $\overline{RAS}$ and $\overline{OE}$ input signals to pull them "High" before or at the same time as the Vcc supply is turned on.
13. Transfer and Serial Read operation can't be perfomed at the same SAM Row simultaneously.

SUMMARY OF 1MByte WRAM ™ BASIC FEATURES AND BENEFITS

Features	256K x 32 WRAM	Benefits
Block Write	8 Columns	High speed FILL, CLEAR, Text with color registers. Maximum 32 byte data transfers (e.g., for 8bpp ; 32 pixels) with plane and byte masking functions
Mixed Modes	LCR + UFBW8 + UFBW8 + ...	All $\overline{CAS}$ falling edge defined cycles (see truth table) can be operated in Mix Modes within Ultra Fast Page cycles.
Color Registers	2	FOREGROUND and BACKGROUND color data in any combination
Mask Register	1	Write-per-bit capability (Bit plane masking)
Latches	4	Aligned BitBLT, SCROLL
Data Bus (Internal)	256	High Bandwith for SCROLL, FILL, BitBLT, Road transfer (with 20ns R/W)
Split SAM	(2)x(128 Bytes)	DISPLAY interface at low cost (Read Transfers only)
Row Length	2048 Bytes	High speed Vertical and Horizontal drawing
Page Cycle Time for External Write(s)/Read(s)	20ns	High speed I/O Interface
Page Cycle Time for External Write(s)/Read(s)	20ns	High performance gain for SCROLL, FILL, BitBLT, and Read transfer operations
Refresh Period	17ms	DISPLAY interface at low cost (Read Transfers only)
Interface	ASYNC	High speed Vertical and Horizontal drawing

BASIC FEATURES/FUNCTIONAL DESCRIPTION

BLOCK WRITE OF 8-COLUMN : BW8

Purpose

To transfer a large block of data (32 bytes max.), which is determined by the 32-bit color register(s) data, to all or any given 32 DRAM plane(s). The BW8 mode is sampled by $\overline{CAS}$ falling edge.

Functional Description

- Each 32-bit of the color register(s) data corresponds to each 32 DRAM planes. Example: D0 corresponds to plane #0 of DRAM array

- A group of column data bits (8 columns) can be written onto any specific 32 DRAM plane(s).

- Any given 32 DRAM plane(s) can be "masked out" through the WPB function for specific plane(s) for protection or overlay application purposes.

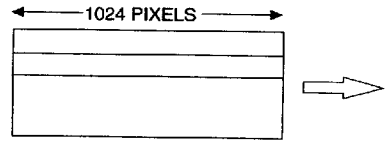
- Byte masking (pixel masking for 8bpp system) function is also provided.

BW8 EXAMPLES

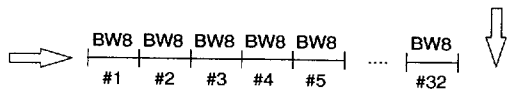
Example #1 (Fill operation from 8bpp system)

The following example will use a BW8 mode to fill two 1024 lines with red color only (assuming red color = 10101010)

Display

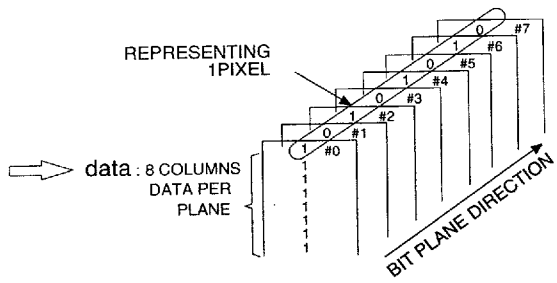


per 1 line requires (32) (BW8)



Each BW8 can transfer maximum 32 bytes ; 32 pixels(8bpp) in one write (20ns) transaction

Each pixel is mapped from 8 DRAM planes in Bit Plane direction per 1 column



The KM4232W259 WRAM has a total of 32 DRAM planes in Bit Plane direction which is comprised of a maximum of 4 pixels from the 1st column of data per DRAM.

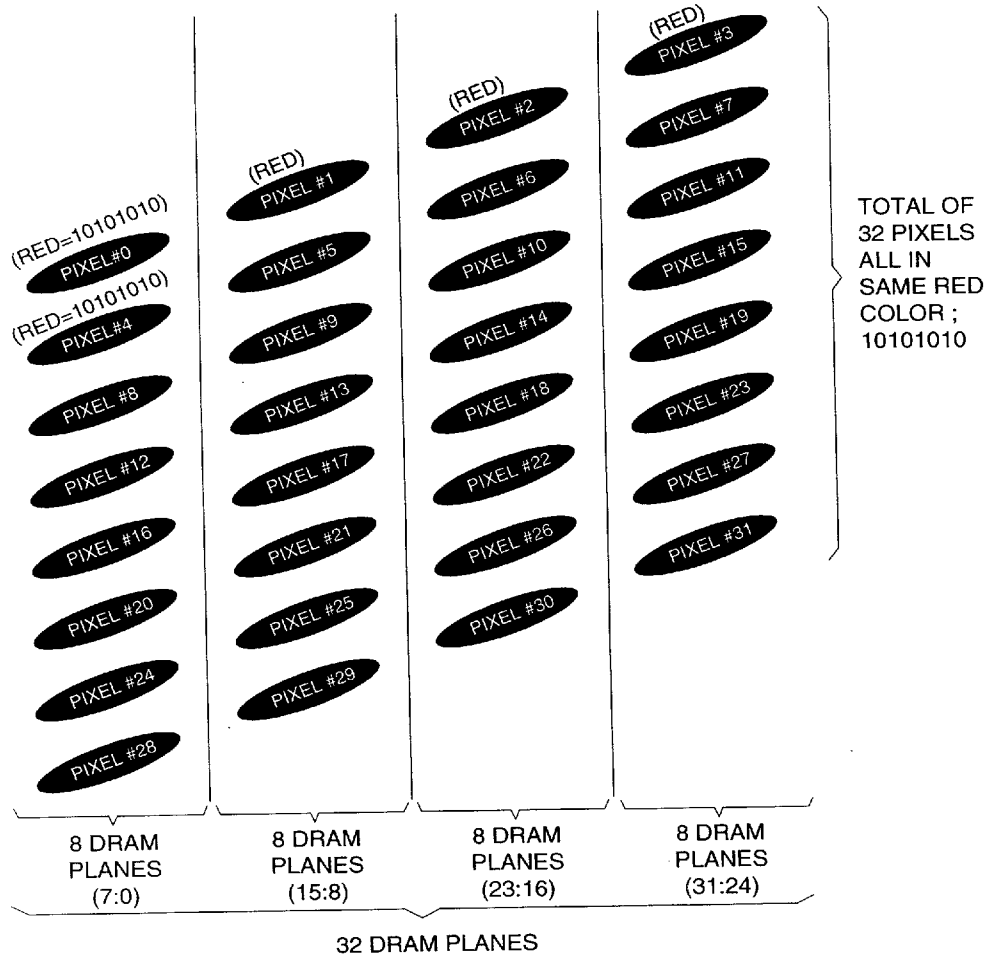
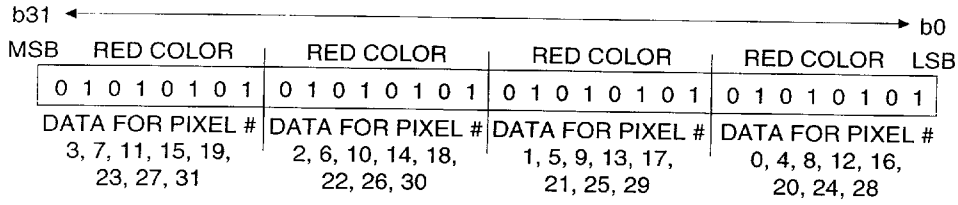


Figure 3. Fill operation from 8bpp System

How Color Registers (0/1) ties to BW8

The color register (#0 or #1) should be loaded with the pixel color data (in this case, red color = 10101010) from 32 I/O pins with a LCR cycle.



Bit #0 of the color register (0 or 1) must tie to DRAM plane #0,
Bit #1 of the color register (0 or 1) must tie to DRAM plane #1,

.
.
.
.

Bit #31 of the color register (0 or 1) must tie to DRAM plane #31,

Cycles reguired for this operation :

LCR (Load color register 0 or 1)
UFBW8
UFBW8

.
.
.
.

UFBW8

Example #2
(Pattern Write Operation from 8bpp System)

The following example uses BW8 mode to write groups of pixel patterns (4 pixels per pattern write) across a partial scan line (for simplicity this example only uses 1 color register mode).

Assuming
RED : 10101010 (R)
GREEN : 01111110 (G)
BLUE : 10000001 (B)
BLACK : 00000000 (NA)

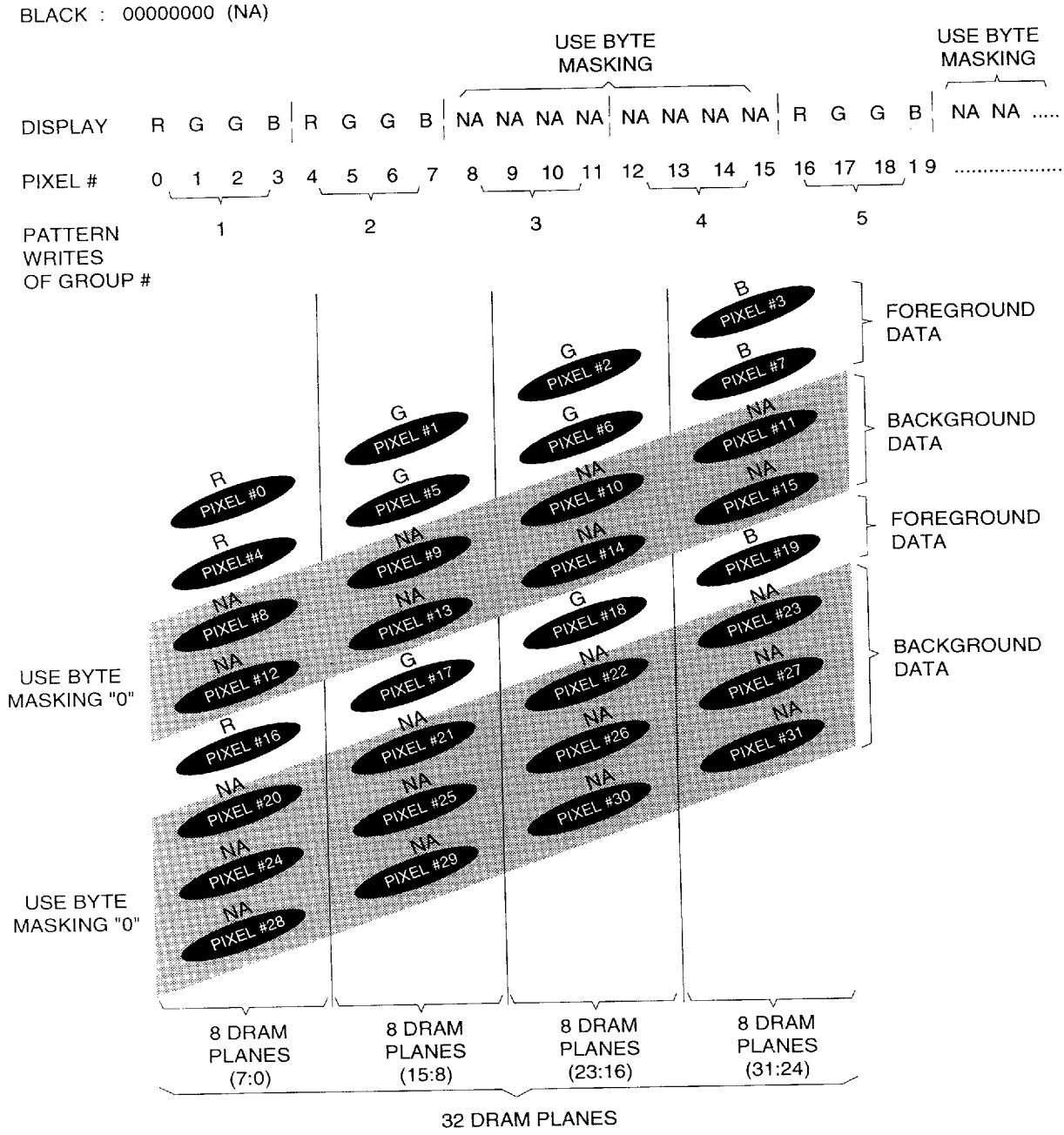
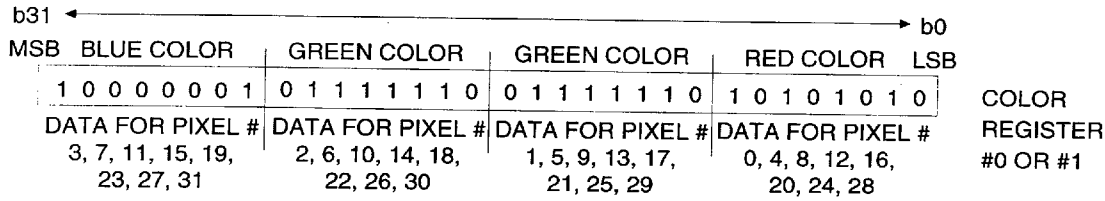


Figure 4. Pattern Write Operation from 8bpp System

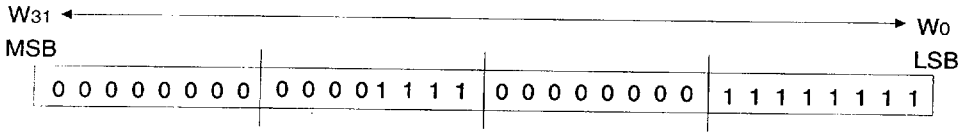
How Color Registers (0/1) ties to BW8

The color register (#0 or #1) should be loaded with the pixel color data (in this case, red color = 10101010) from 32 I/O pins with a LCR cycle.



Masking out Pixel # <15:8> and # <31:20>

Use byte masking (8bpp => pixel masking) function from BW8 mode at the falling edge of $\overline{CAS}$.
In this BW8 cycle with byte masking, the 32-bit Data Write Mask (W_0-W_{31}) should be provided as follows.



1 => Enable the Byte write
0 => Disable the Byte write
W<7:0> enable the write buffers ; allow pixel<7:0> not to be masked.
W<19:16> enable the write buffers ; allow pixel<19:16> not to be masked.
W<15:8> & W<31:20> disable the write buffers ; allow pixel #<15:8> & #<31:20> to be masked.

Each of these bits can be used to mask ("0") or not mask ("1") the whole 8-bit pixel data.

Use BW8 mode to write R G G B pixels data (foreground data).

Repeat the above steps to write NA NA NA NA pixel data (background data)

Cycles required for this operation :

(Foreground R G G B)
- LCR
- Byte mask info // UFBW8

(Background NA NA NA NA)
- LCR
- Byte mask info // UFBW8

Example #3 : (Random Pattern Write Operation from 8bpp System)

The following example uses BW8 mode to write a "RED CROSS" across a portion of 3 scan lines with one color register ; (can also be done by using ultra fast write cycle for the "RED CROSS" or with 2 color register mode for faster drawing).

Assuming RED ; 10101010 (R)
WHITE ; 11110000 (W)

DISPLAY	W	W	W	W	W	W	W	W	R	R	R	X	W	W	W	W	W	.....		
	W	W	W	W	W	R	R	R	R	R	R	R	R	R	W	W	W	.....		
	W	W	W	W	W	W	W	W	R	R	R	W	W	W	W	W	W	.....		
PIXEL #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	.....	31	(FOR SCAN #1)
	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	.....	63	(FOR SCAN #1)
	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	.....	95	(FOR SCAN #1)

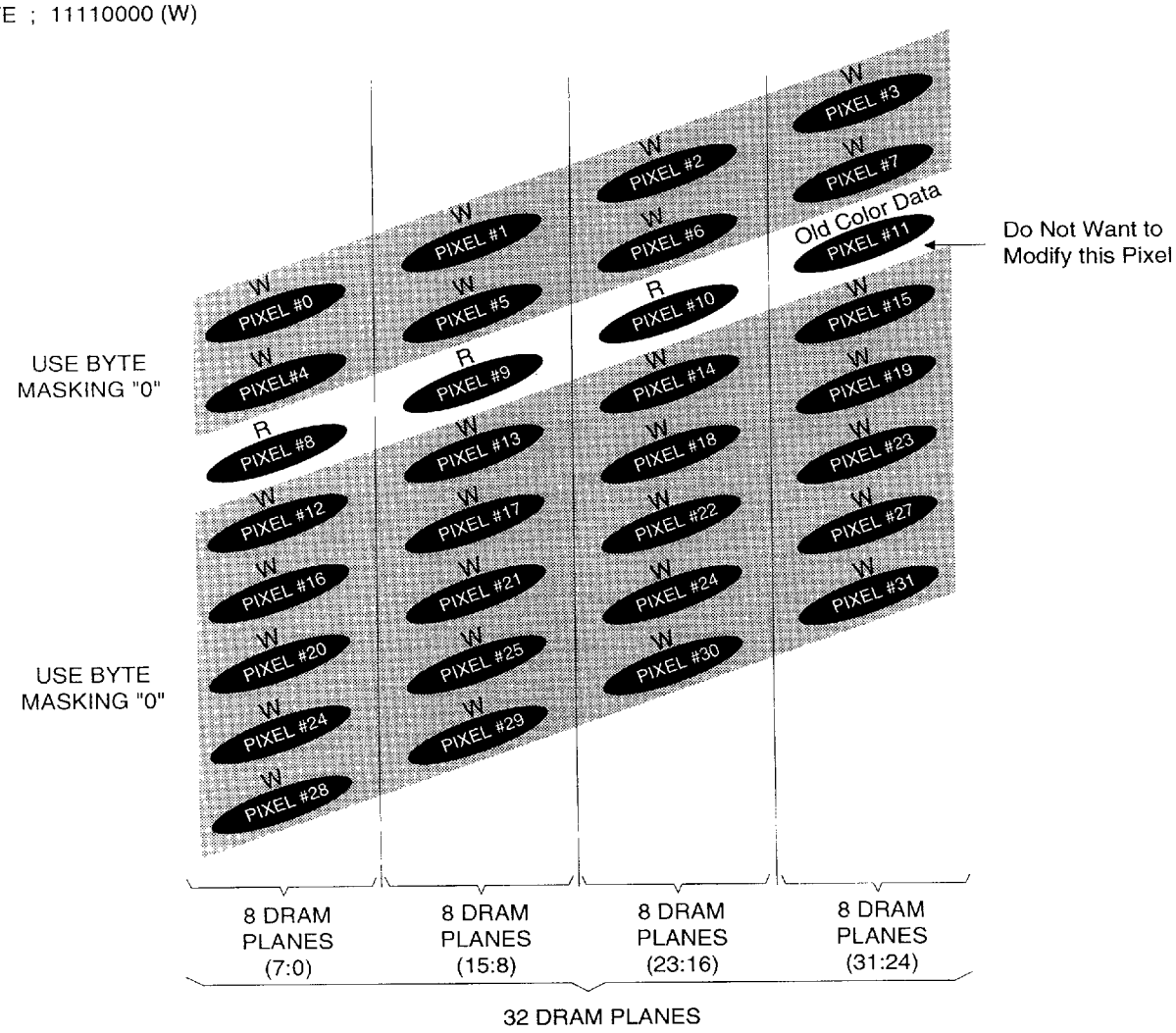
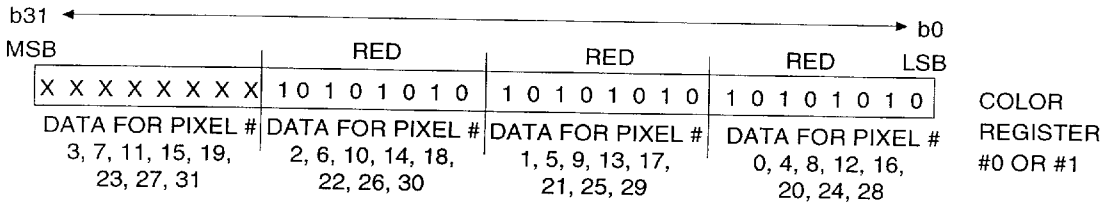


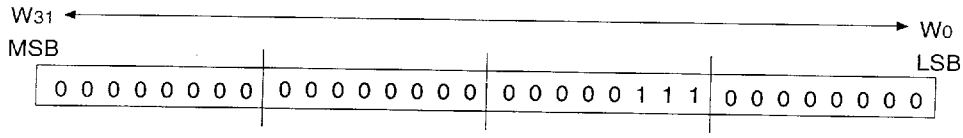
Figure 5. Random Pattern Write Operation from 8bpp System

Load the color register (#0 or #1) with the following infomation:



Pixel # <7:0> and # <31:11> masked out

Use Byte masking function BW8 mode (pixel masking for 8bpp system) to mask at the falling edge of $\overline{CAS}$; 32-bit Data Write Mask (W_0-W_{31}) should be provided as follows:



0 => Disable the Byte write
1 => Enable the Byte write

this pixel masking data (byte masking data) should be done from BW8 cycle.

Cycles required for this operation:

LCR cycle for color register 0
Byte masking information // UFBW8
-- **Use the same methodology to fill out "W" color data for pixel # <7:0> and # <31:12> on scan line #1.**

-- **Repeat the above steps for the next 2 scan lines of information.**

Example #3 : (Random Pattern Write Operation from Block Write 2 Color Registers.)

The following example uses BW8 mode to write a "RED CROSS" across a portion of 3 scan lines with 2 color register .

Assuming

RED ; 10101010 (R)
WHITE ; 11111111 (W)

DISPLAY	W	W	W	W	W	W	W	W	R	R	R	W	W	W	W	W	W		
	W	W	W	W	W	R	R	R	R	R	R	R	R	R	W	W	W		
	W	W	W	W	W	W	W	W	R	R	R	W	W	W	W	W	W		
PIXEL #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	31	(FOR SCAN #1)
	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	63	(FOR SCAN #2)
	64	65	66	67	70	71	72	73	74	75	76	77	78	79	80	81	82	95	(FOR SCAN #3)

FOR SCAN LINE #1

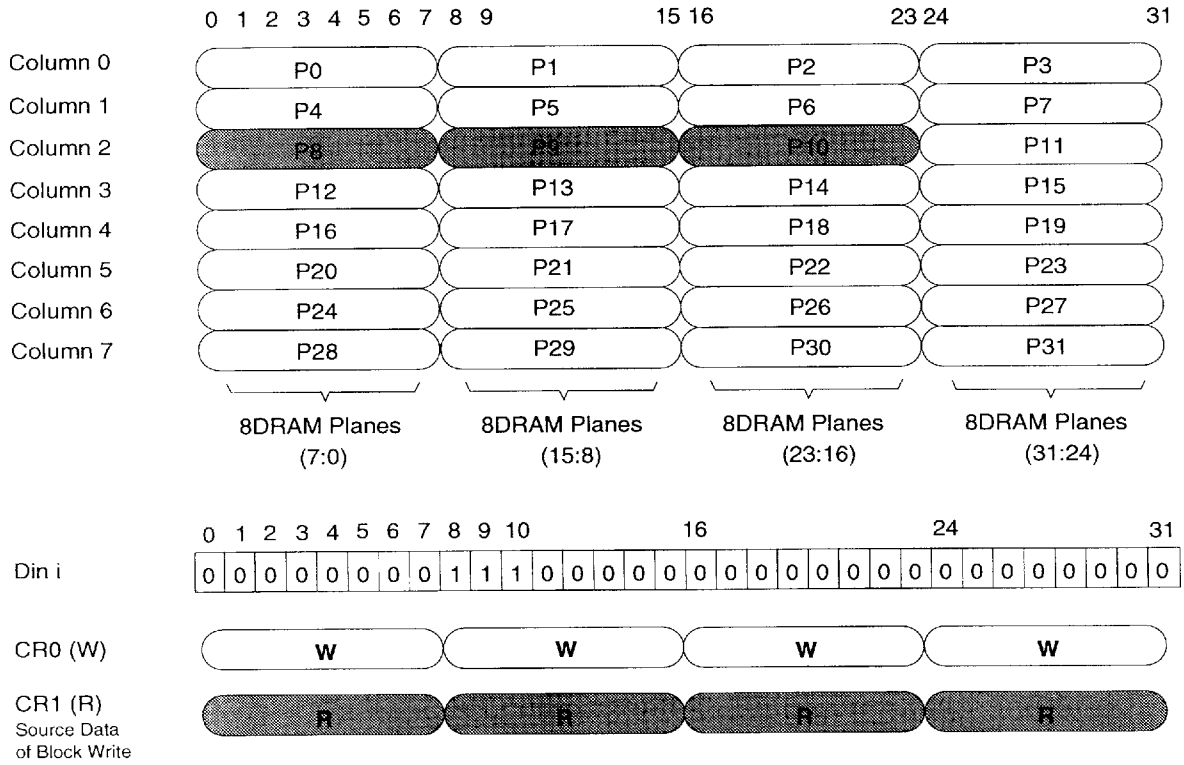
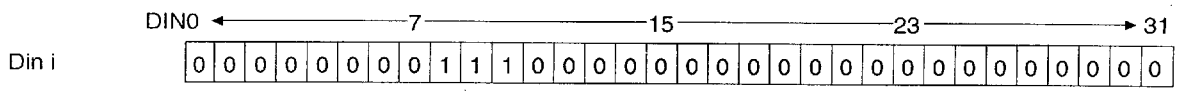


Figure 6. Example of BW8 Using Both Color Registers

Cycles required for this operation:
- LCR cycle for Color register 0 (Load White Color)
- LCR cycle for Color register 1 (Load Red Color)
- BW8 cycle with DINi information

Date for Scan Line #1



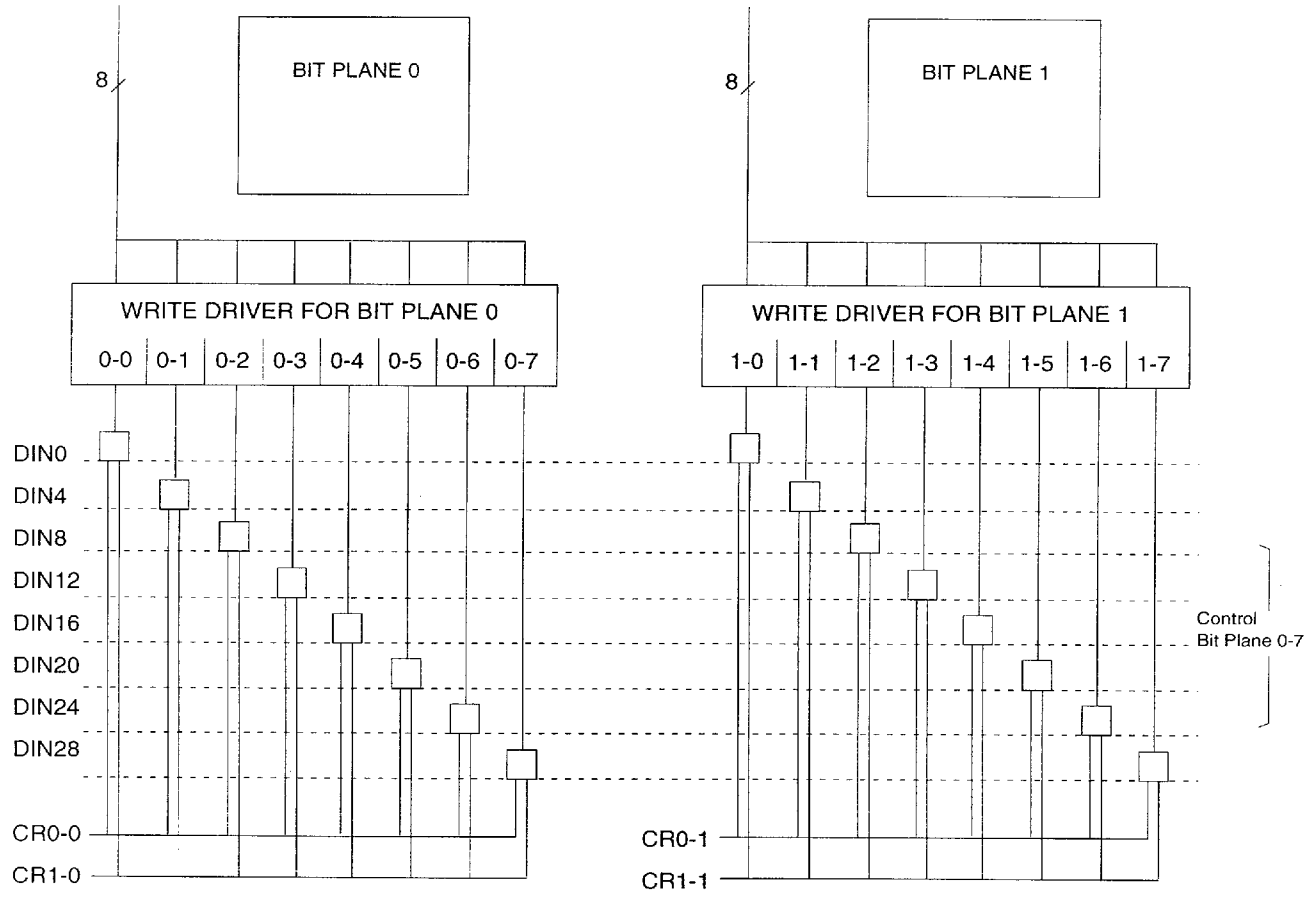


Figure 7. Block Diagram for BW8 with 2 Color Regisrers

MASK OPERATION

The WRAM offers data masking in the following operation.

- Nomal Ultra Fast Page Mode Write Cycle
- Block Write Mode
- Internal data block move from Latch to DRAM

MASK REGISTER (WPB Mask)

Loading the mask register can be performed in two ways:

a) $\overline{RAS}$ controlled. At the falling edge of $\overline{RAS}$, if $\overline{OE}$="1", then DQi will update mask register

b) The $\overline{CAS}$ - controlled LMR cycle also updates the mask register.

Each bit of the mask register (=MRi) Directly controls a corresponding bit plane.

MR0 -> Bit Plan 0,
MR1 -> Bit Plan 1.....
MR31 -> Bit Plan 31.

Each bit enables write if "1", and disables write if "0".

PIXEL (BYTE) MASK Operation

This operation is active for BW8 cycles or Latch to DRAM cycle. Each Pixel can be masked by the value of DQi at $\overline{CAS}$ falling edge.

Pixel0 - DQ0, Pixel1-DQ1..., Pixel31 - DQ31
DQi set to "0" disables pixel
DQi set to "1" enables pixel

BYTE ENABLE Control

$\overline{BE}$0 -3 are sampled at $\overline{CAS}$ falling edge. Each Byte Enable Line ($\overline{BE}$0-3) disables the corresponding byte to be written if set to "1", if set to "0" each Byte Enable line enables the corresponding byte.

$\overline{BE}$0 Controls Bit Plane 0:7
$\overline{BE}$1 Controls Bit Plane 8:15
$\overline{BE}$2 Controls Bit Plane 16:23
$\overline{BE}$3 Controls Bit Plane 24;31

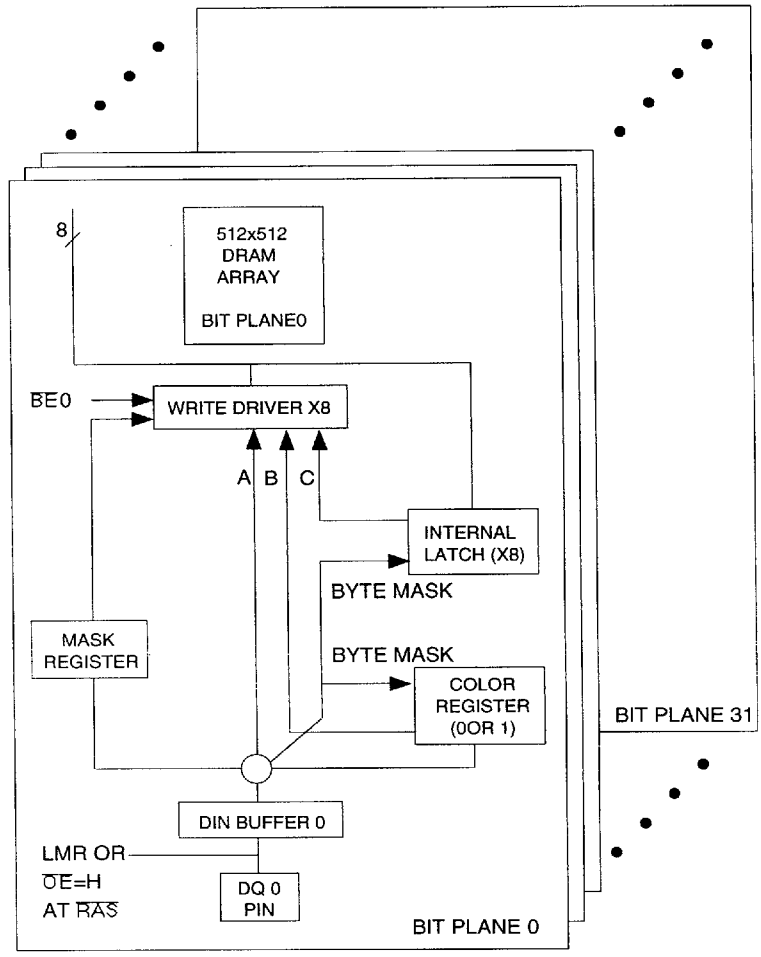


Figure 8. Block Diagram of data path for all of write operation.

In figure 8, "A" refers to a data path in a normal write mode ; "B" refers to Block Write ; "C" refers to an internal data block move.

The block diagram illustrates how each WRAM plane relates to the corresponding register bit, and I/O pin. It also illustrates the data path for the following WRAM cycle :

a) Ultra fast page write cycle.
b) Block Write cycle
c) Internal data block move cycle.

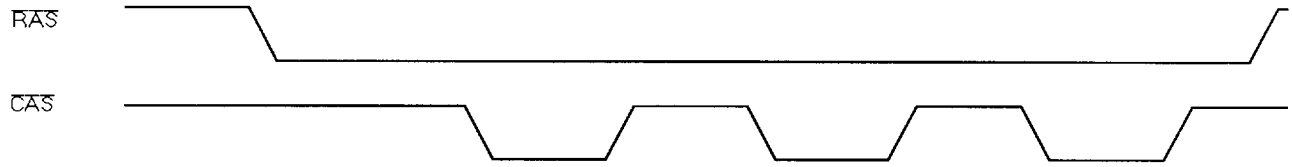
Ultra Fast Page Mode Write Operation (Bit Plane Mask)

In figure 9, the example initializes MRi data at the $\overline{RAS}$ falling edge, after which the first write operation is executed with the Bit Plane mask information. Change of MRi data occurs through an LMR cycle, after which the new Bit Plane Mask information is used for the second write operation.

BW8 Operation with Pixel and Bit Plane Mask

Figure 10 shows an example of Block Write 8 operation with one color register. To execute this operation, three cycles are performaed sequentially :

LCR cycle = Load the color register data
LMR cycle = Load the bit plane mask data
BW8 cycle = Write the color register data to the DRAM array cell by pixel (Byte) mask



	LOAD MASK REGISTER	1ST WRITE	LMR CYCLE	2ND WRITE
DQ0	0	1	1	1
DQ1	1	1	0	1
DQ2	0	1	1	1
DQ3	1	1	0	1
DQ4	0	1	1	0
DQ5	1	1	0	0
DQ6	0	1	1	0
DQ7	1	1	0	0

	RESULTS OF WRITING							
	Bit Plane 0	Bit Plane 1	Bit Plane 2	Bit Plane 3	Bit Plane 4	Bit Plane 5	Bit Plane 6	Bit Plane 7
PREVIOUS DATA	0	0	0	0	0	0	0	0
AFTER 1ST WRITE	0	1	0	1	0	1	0	1
AFTER 2ND WRITE	1	1	1	1	0	1	0	1

Note) ▒ : Data not change

Figure 9. Example of Ultra Fast Page Mode Write Operation (Bit Plane Mask)

TIMING SEQUENCE

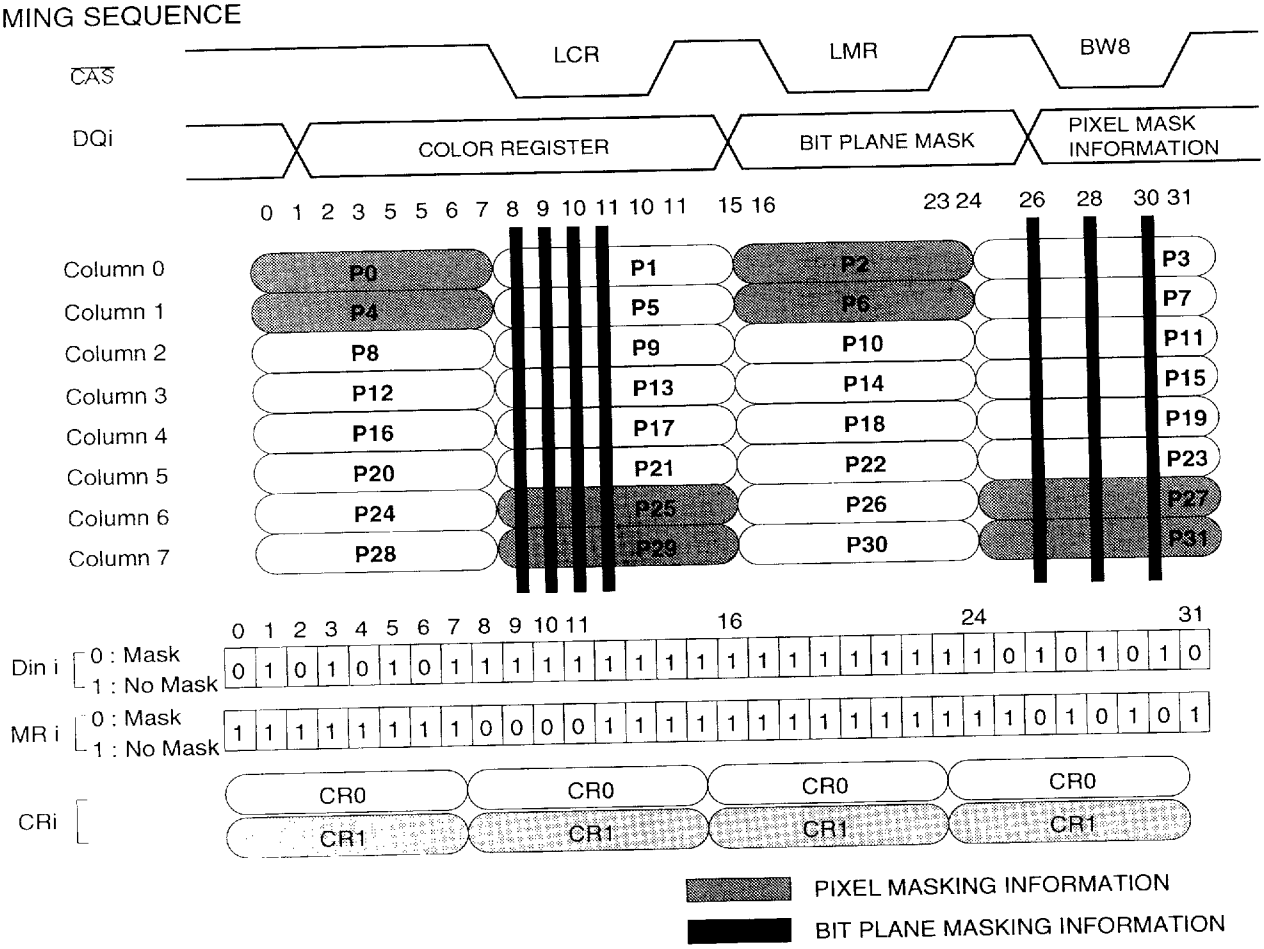


Figure 10. Example of a BW8 Operation with Pixel and Bit Plane Masking

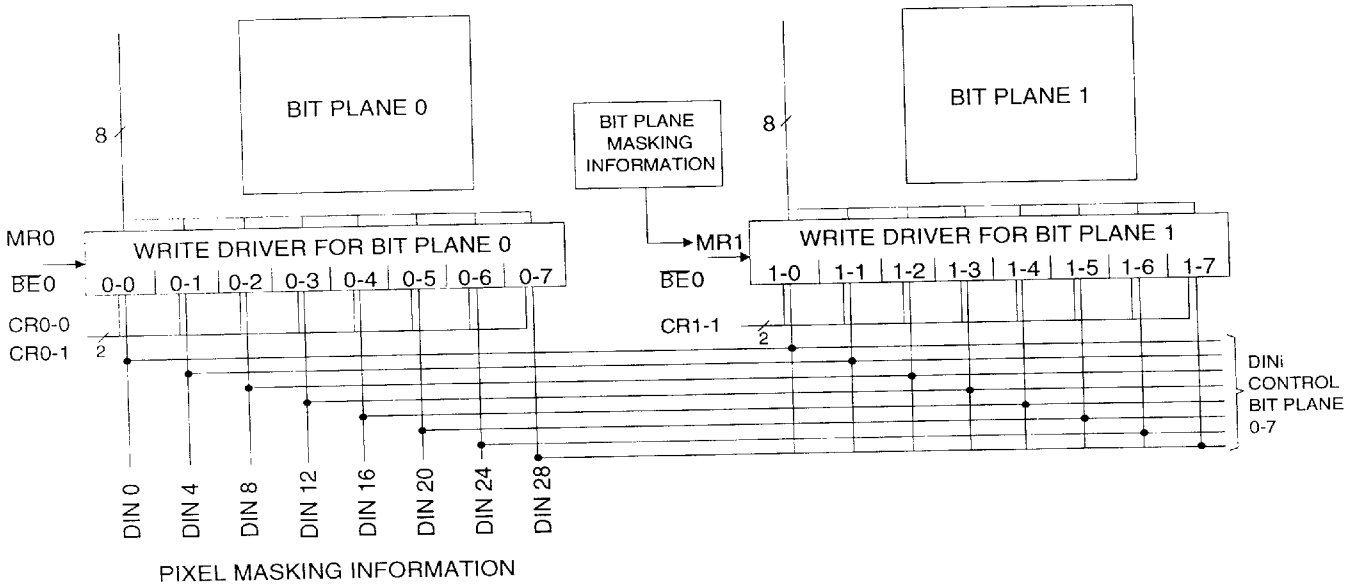


Figure 11. Block Diagram for BW8 With Pixel and Bit Plane Mask

SAM TRANSFER OPERATION

A Transfer operation is initiated when DSF_0 is "L", DSF1 is "H", and DSF_2 is "L" at $\overline{CAS}$ falling edge. 32 bytes of data transfers from DRAM to SAM via a 256-bit internal buses within 20ns. When the transfer cycle is executed, the internal transfer pointer addresses the SAM register that contains the data transfered from the RAM. The column addresses A_3 to A_8 is the source address of the 32 bytes of data to be transferred to the SAM register.

The total SAM size is 256 bytes, consisting of the 8 split register. Each split register has a size of 32 bytes, which is the same as the internal bus size that fills it by one transfer cycle. To fill a whole SAM register, 8 transfer cycles are required (Figure 12).

There are two types of transfer cycles : Split Read Transfer cycle (SRT) and Split Read Transfer cycle with Reset (SRTR). The status of coulmn address (A_0) at the falling edge of $\overline{CAS}$ determines which type of transfer cycle(SRT or SRTR) is executed. CA_0 set to "0" selects an SRT cycle and CA_0 set to "1" selects the SRTR cycle.

The Transfer pointer which addresses the position in the SAM register is a wrap-around counter and increments by 1 each transfer cycle. The SAM register is reset to the first row position (the first row of the SAM register) by the SRTR cycle. On the first SRT cycle after power up also performs the same reset function for the transfer pointer.

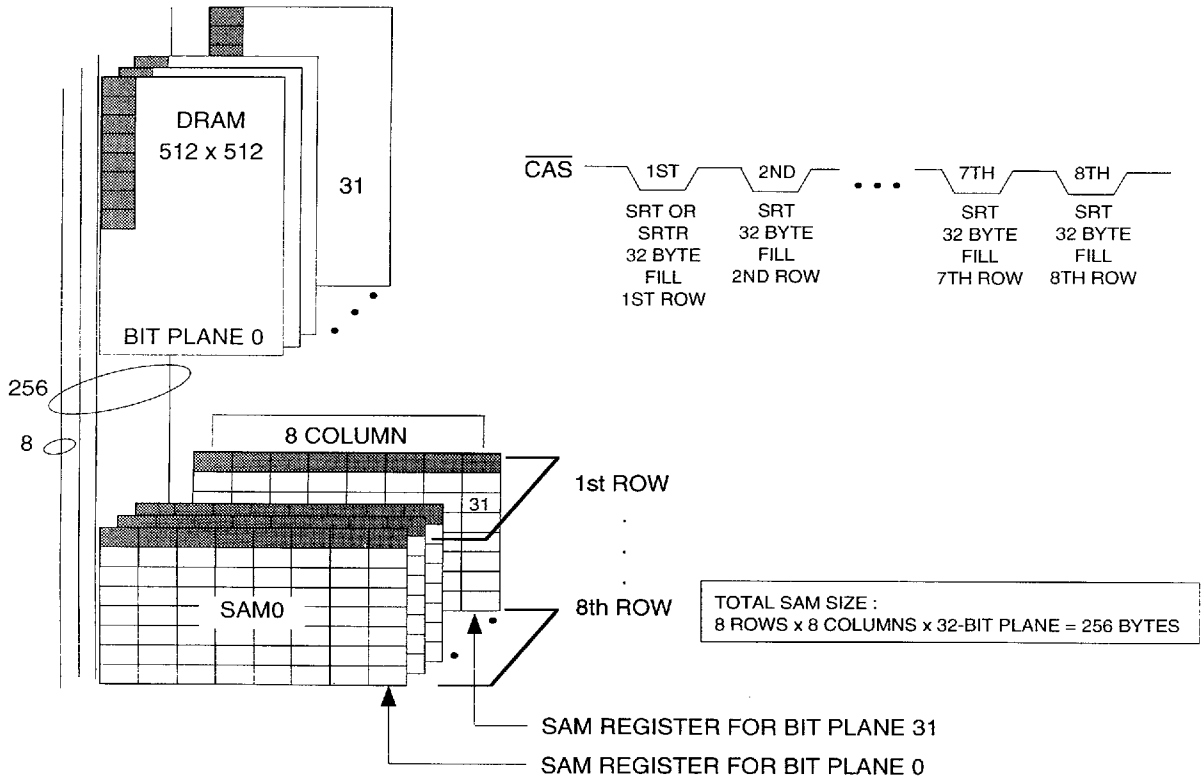


Figure 12. Example of Transfer Cycle.

Serial Read Operation

While transferring the DRAM data to SAM, users can continuously read out SAM data to the serial outputs from different rows of the SAM. There are 16 serial outputs provided on the serial port. The on-chip 32 SAM outputs which correspond the 32 DRAM bit planes, are shifted out through an on-chip 2:1 MUX to the SQ_0-SQ_{15} pins(see Figure 13)

- A maximum of 2 pixels are read out from the WRAM at the same time for 8bpp system.

- A maximum of 1 pixel is read out from the WRAM at the same time for 16bpp system.

- A maximum of 1/2 pixel is read out from the WRAM at the same time for 32bpp system.

The DRAM plane #<15:0> ties to one SQ read, while the DRAM plane #<31:16> ties to another SQ read on the next serial read cycle.

The SAM address pointer is the SAM counter output.

The SAM counter is n-bit up-counter and wraps around by the internal operation, it is reset by the SRTR cycle and 1st SRT right after Power-up.

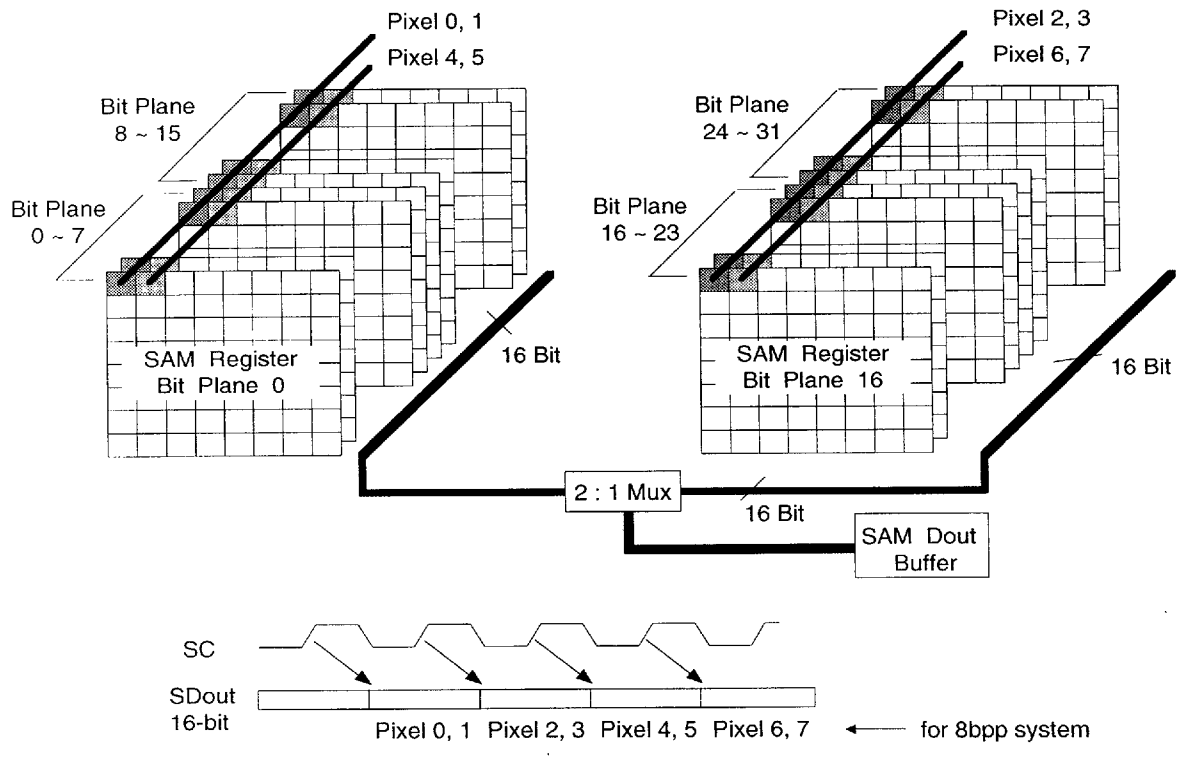
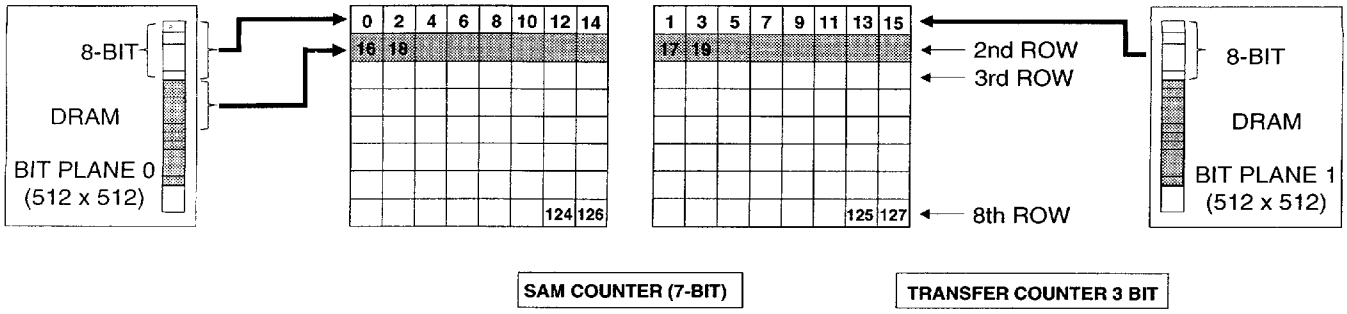


Figure 13. Functional Block Diagram of Serial Read



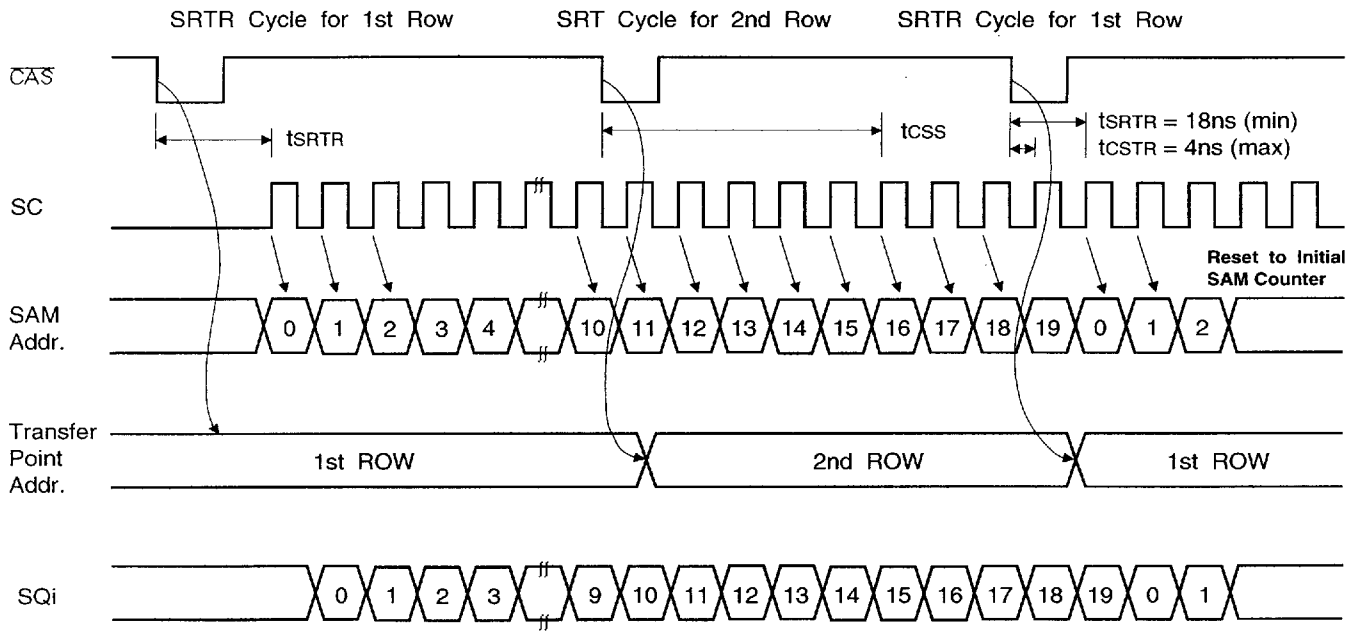


Figure 14. Example of SAM Operation

Figure 14 illustrates the operation of the transfer cycle and the serial read cycle. The first $\overline{CAS}$ cycle performs the following :

SRTR cycle transfers the 8-bit column data of selected row to the 1st row of SAM register. This cycle performs a reset operation to the transfer counter to address the first row, and resets the SAM counter to address "0" of the first row of the SAM register.

The second $\overline{CAS}$ cycle performs the following :

The SRT cycle transfers the 8-bit column data of selected row to the second row of SAM register. When the SRT cycle is performed, the t_{CSS} is a minimum 6 SC cycle delay from SRT cycle to the first SC clock for reading the data from that SRT cycle.

The third CAS cycle performs the following :

The SRTR cycle resets the transfer counter and SAM counter. The transfer counter points to the first row of SAM, and the SAM counter addresses "0" position of the 1st row of SAM.

When the SRTR cycle is executed, t_{SRTR} and t_{CSTR} parameters must be satisfied in order to read the transferred data without delay (see Figure 15). t_{SRTR} and t_{CSTR} are critical AC parameters to ensure the proper operation of SRTR cycle. The difficulty of controlling t_{SRTR} and t_{CSTR} is similar to the difficulty of controlling t_{TSD} and t_{TSL} in a Real-Time Read transfer cycle of VRAM.

EXAMPLE

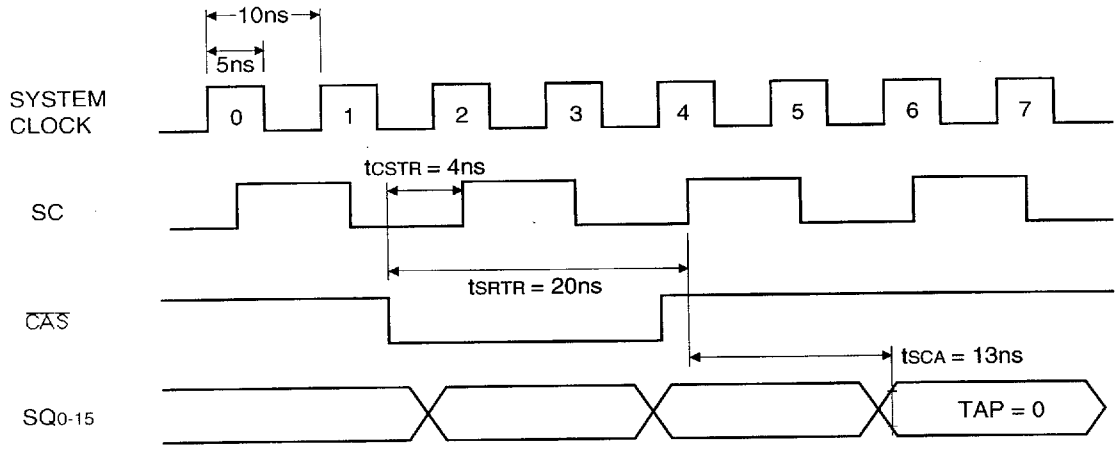
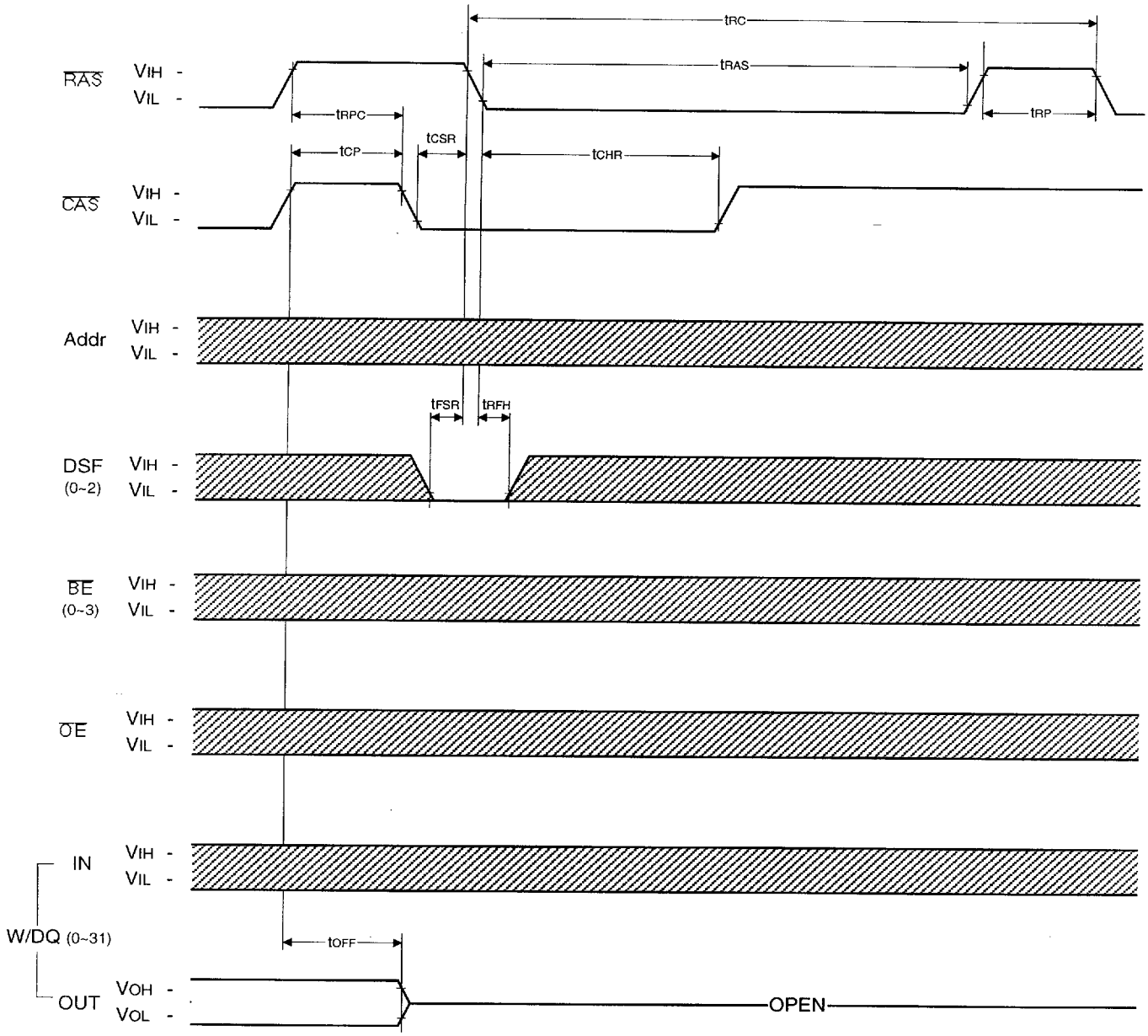


Figure 15. Examples of System Clock Condition to Perform SRTR Cycle [t_{SRTR}=18ns (min.), t_{CSTR}=4ns(max.)]

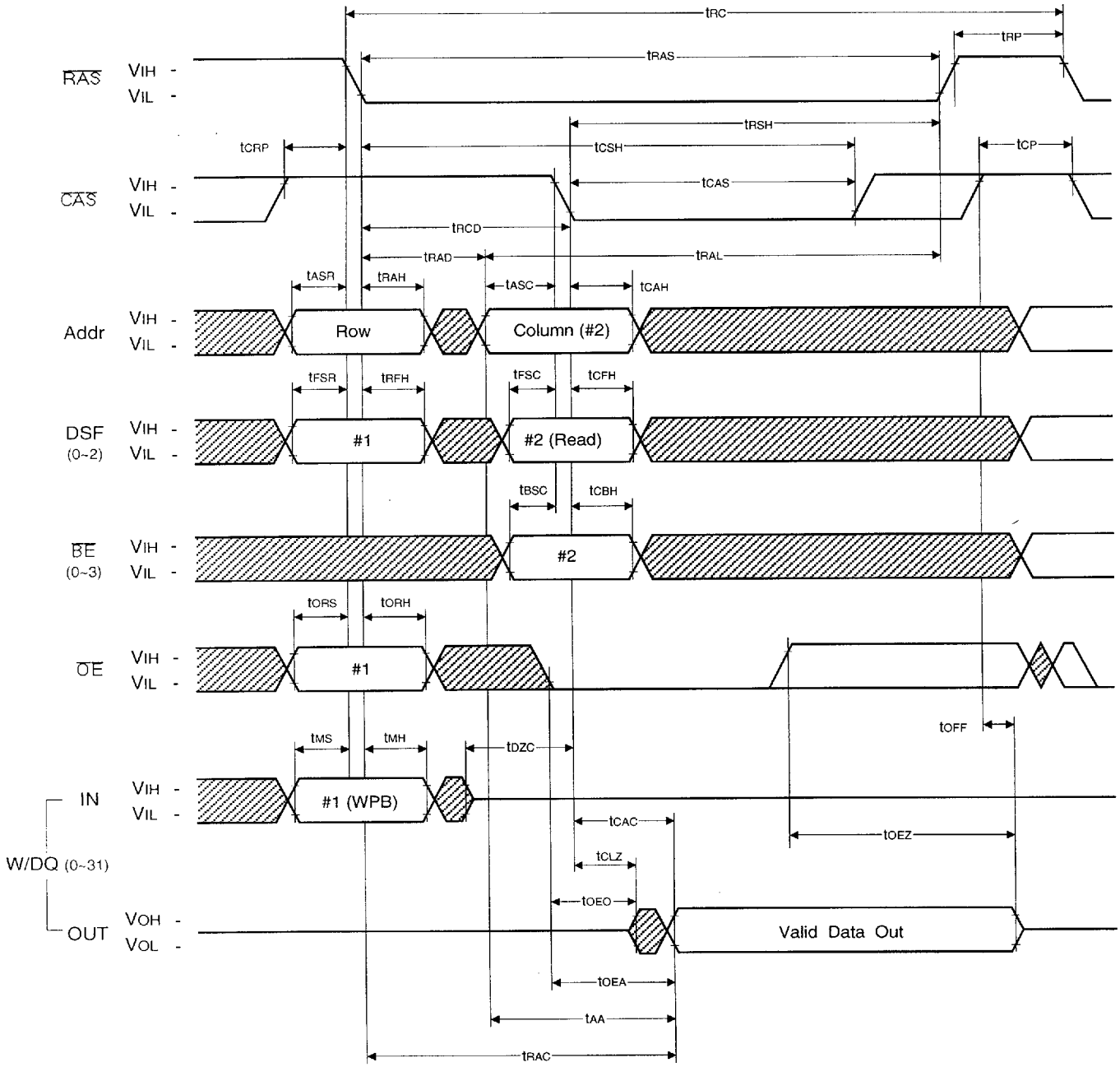
TIMING DIAGRAMS (continued)

RESET CYCLE



: Don't Care

TIMING DIAGRAMS
READ CYCLE (DRAM)

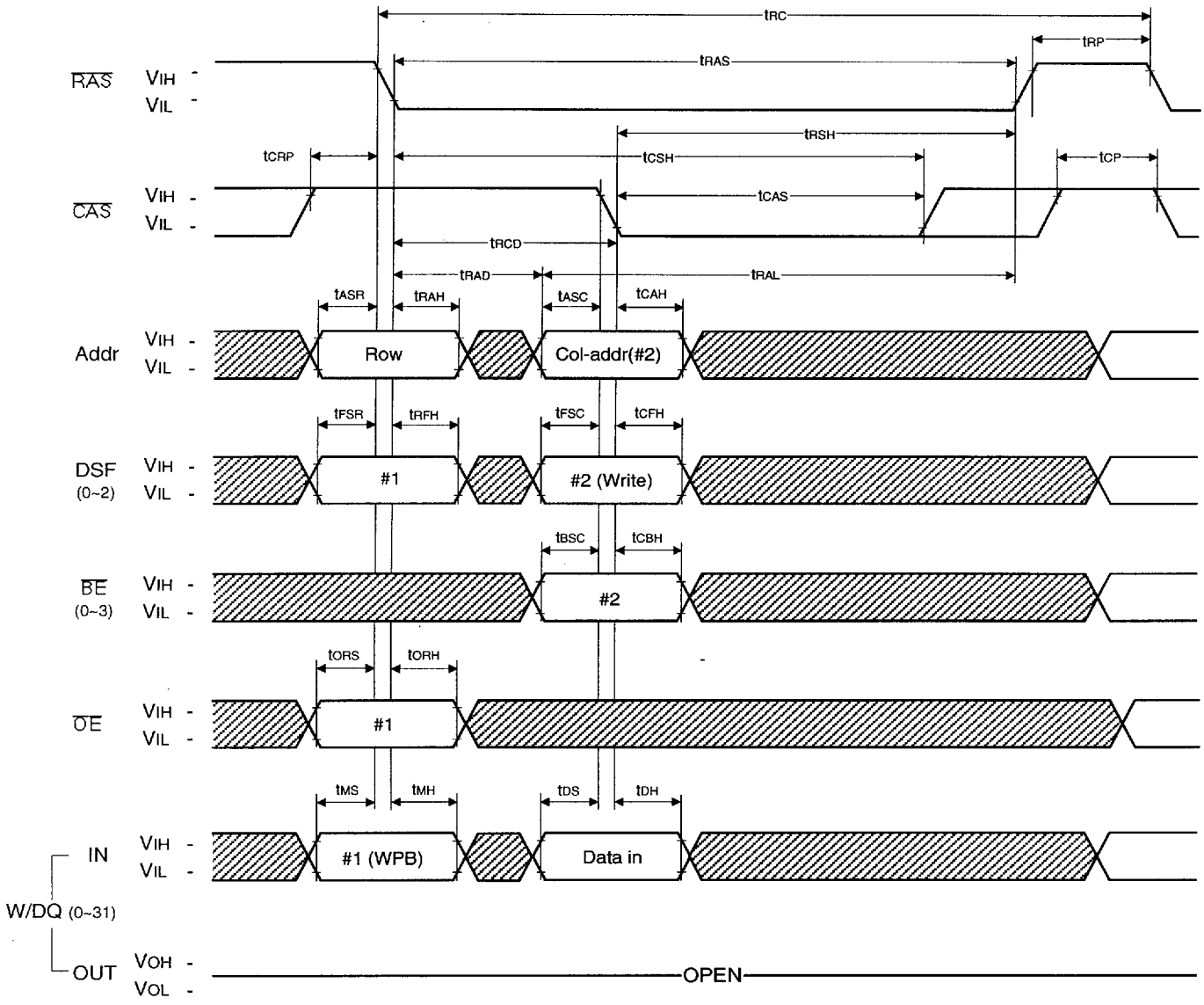


*Note ; #1,#2 : Refer to " Truth Tables"

: Don't Care

TIMING DIAGRAMS (continued)

WRITE/LOAD CYCLE (DRAM, Color/Mask Register)

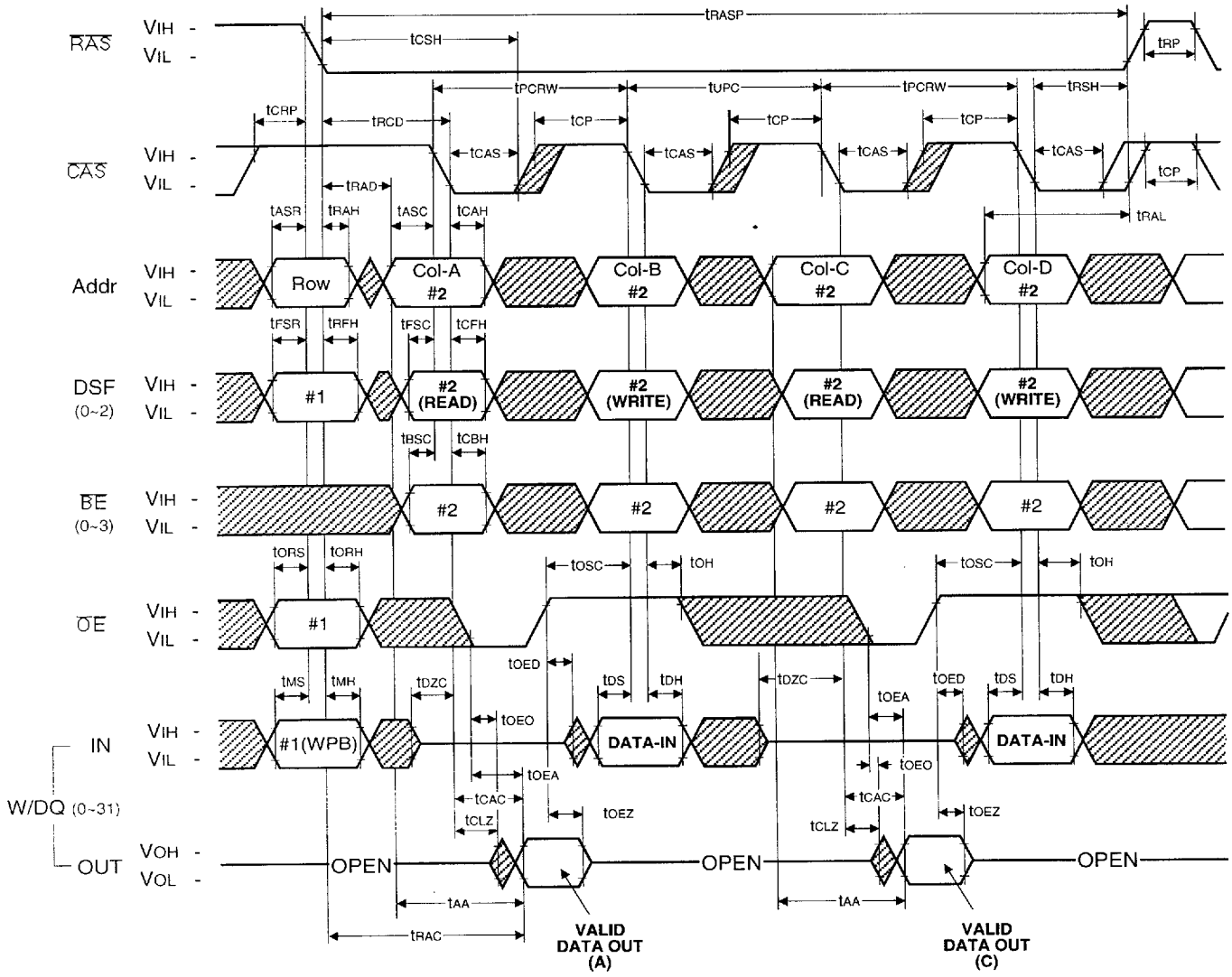


*Note ; #1,#2 : Refer to " Truth Tables"

: Don't Care

TIMING DIAGRAMS (continued)

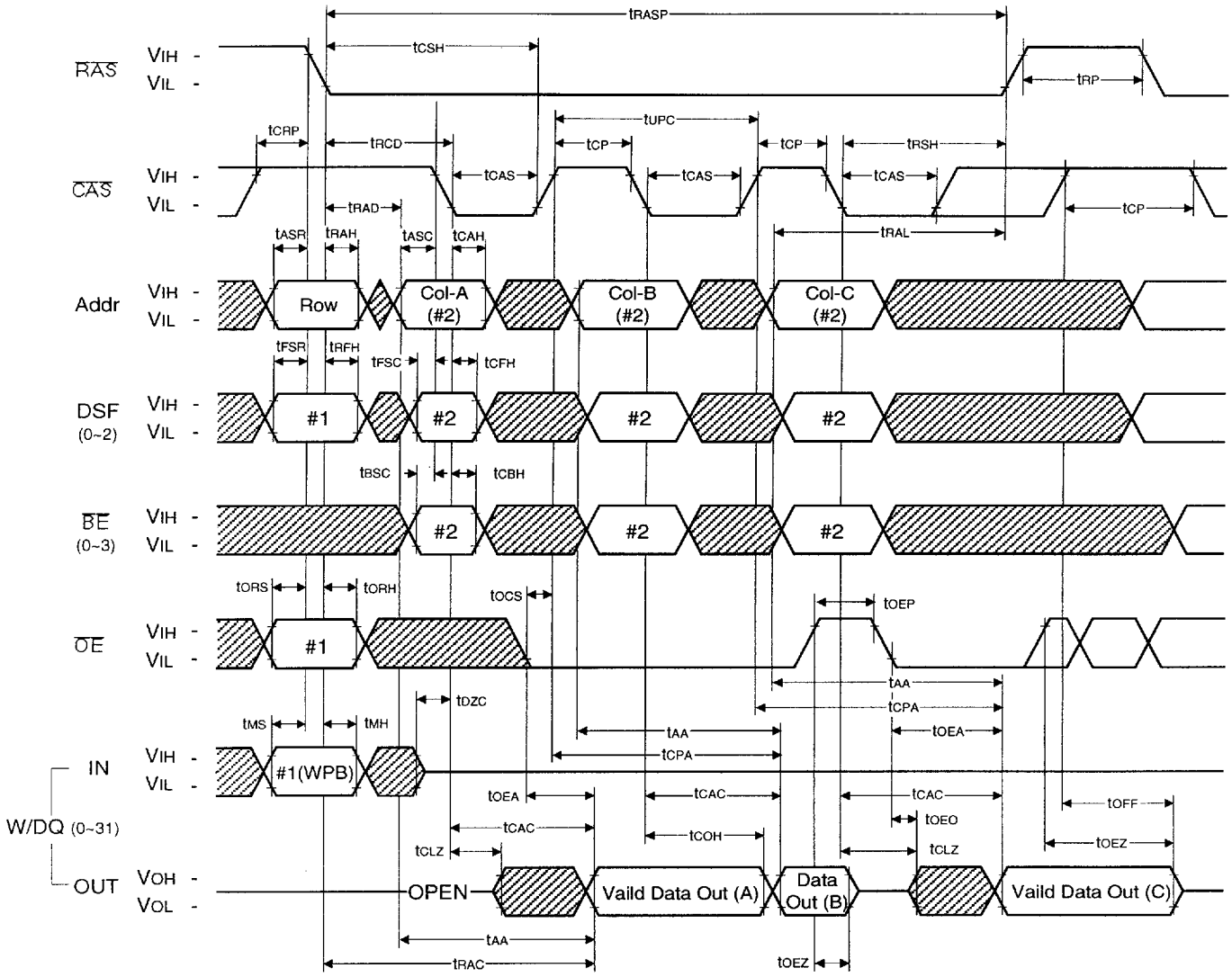
READ-WRITE CYCLE (DRAM, Color/Mask Register)



*Note ; #1,#2 : Refer to " Truth Tables"

: Don't Care

TIMING DIAGRAMS (continued)
ULTRA FAST PAGE READ CYCLE (DRAM)

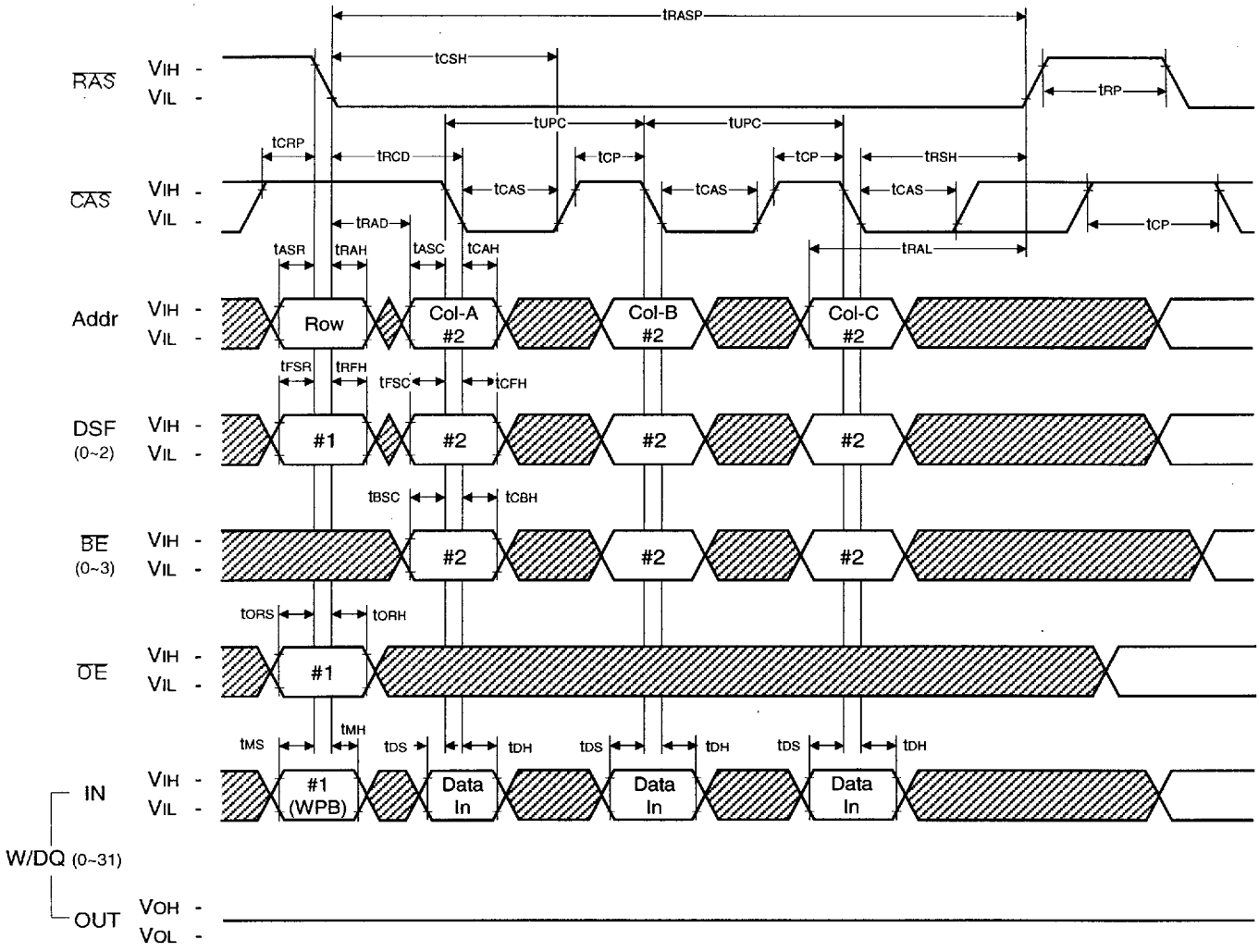


*Note ; #1,#2 : Refer to " Truth Tables"

: Don't Care

TIMING DIAGRAMS (continued)

ULTRA FAST PAGE WRITE/LOAD CYCLE (DRAM, Color/Mask Register)

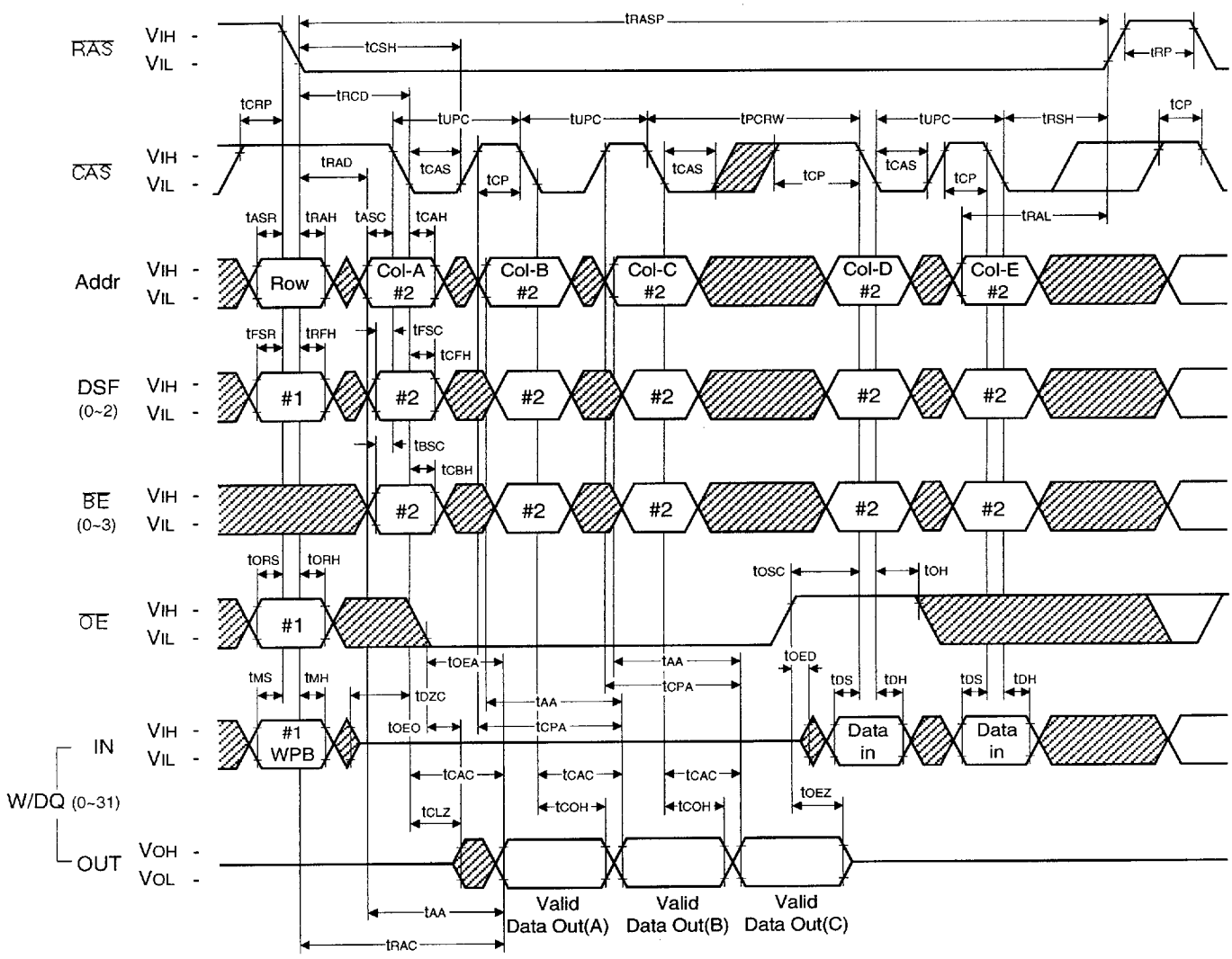


*Note ; #1,#2 : Refer to " Truth Tables"

: Don't Care

TIMING DIAGRAMS (continued)

ULTRA FAST PAGE READ-WRITE/LOAD CYCLE (DRAM, Color/Mask Register)

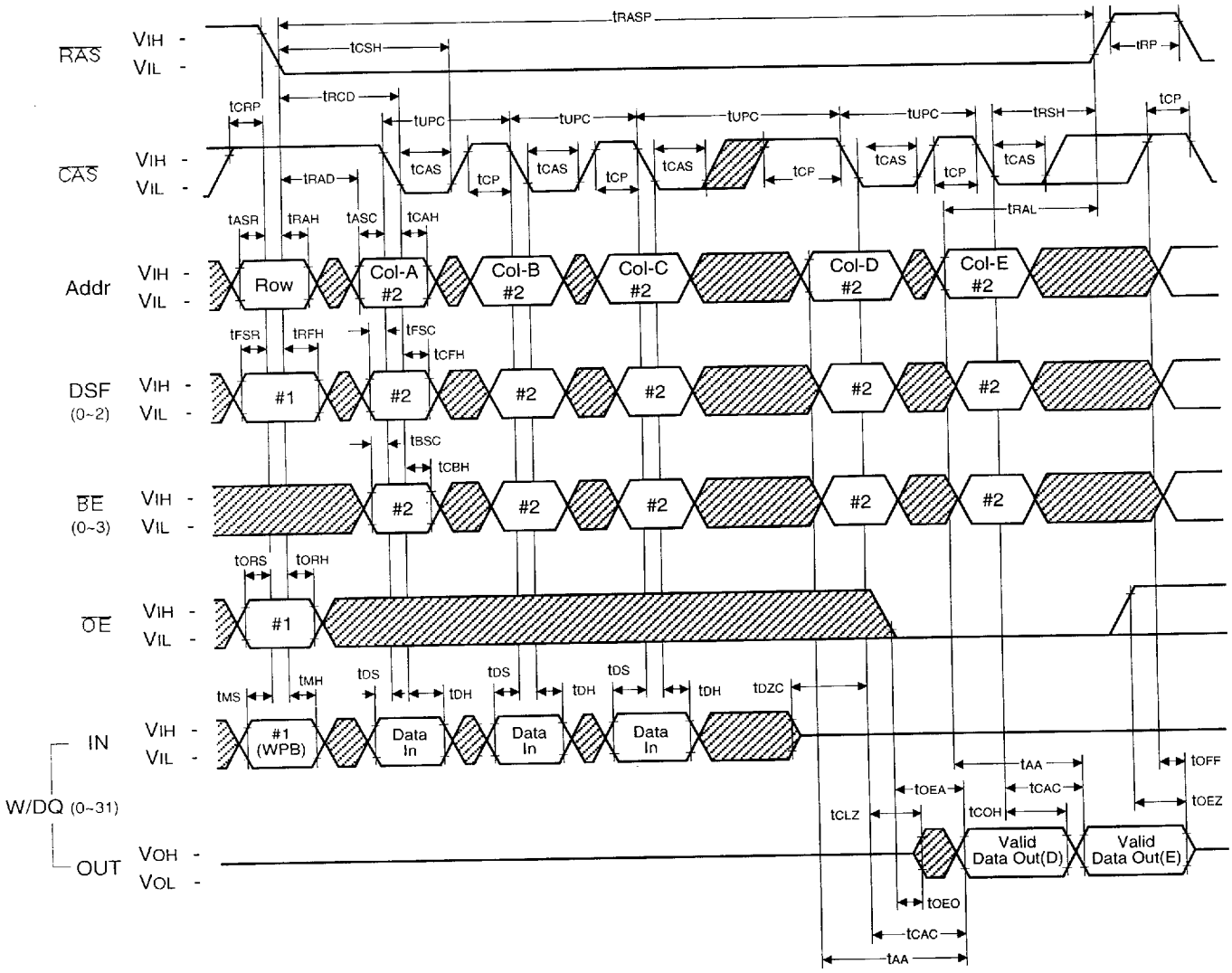


*Note ; #1,#2 : Refer to " Truth Tables"

: Don't Care

TIMING DIAGRAMS (continued)

ULTRA FAST PAGE WRITE/LOAD-READ CYCLE

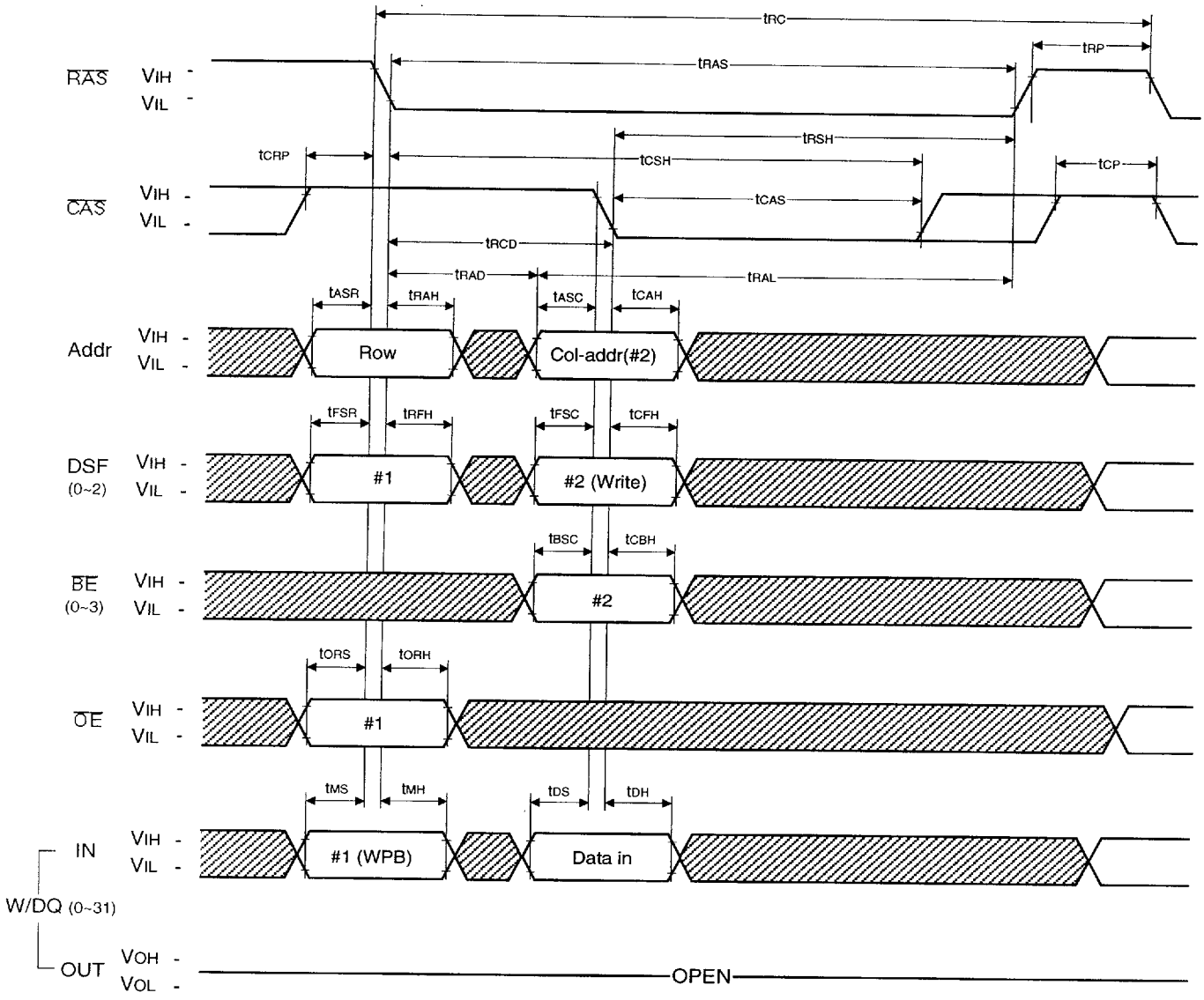


*Note ; #1,#2 : Refer to " Truth Tables"

: Don't Care

TIMING DIAGRAMS (continued)

INTERNAL OPERATIONAL CYCLE (UFBR, UFBWL, UFBW8 SRT, SRTR)

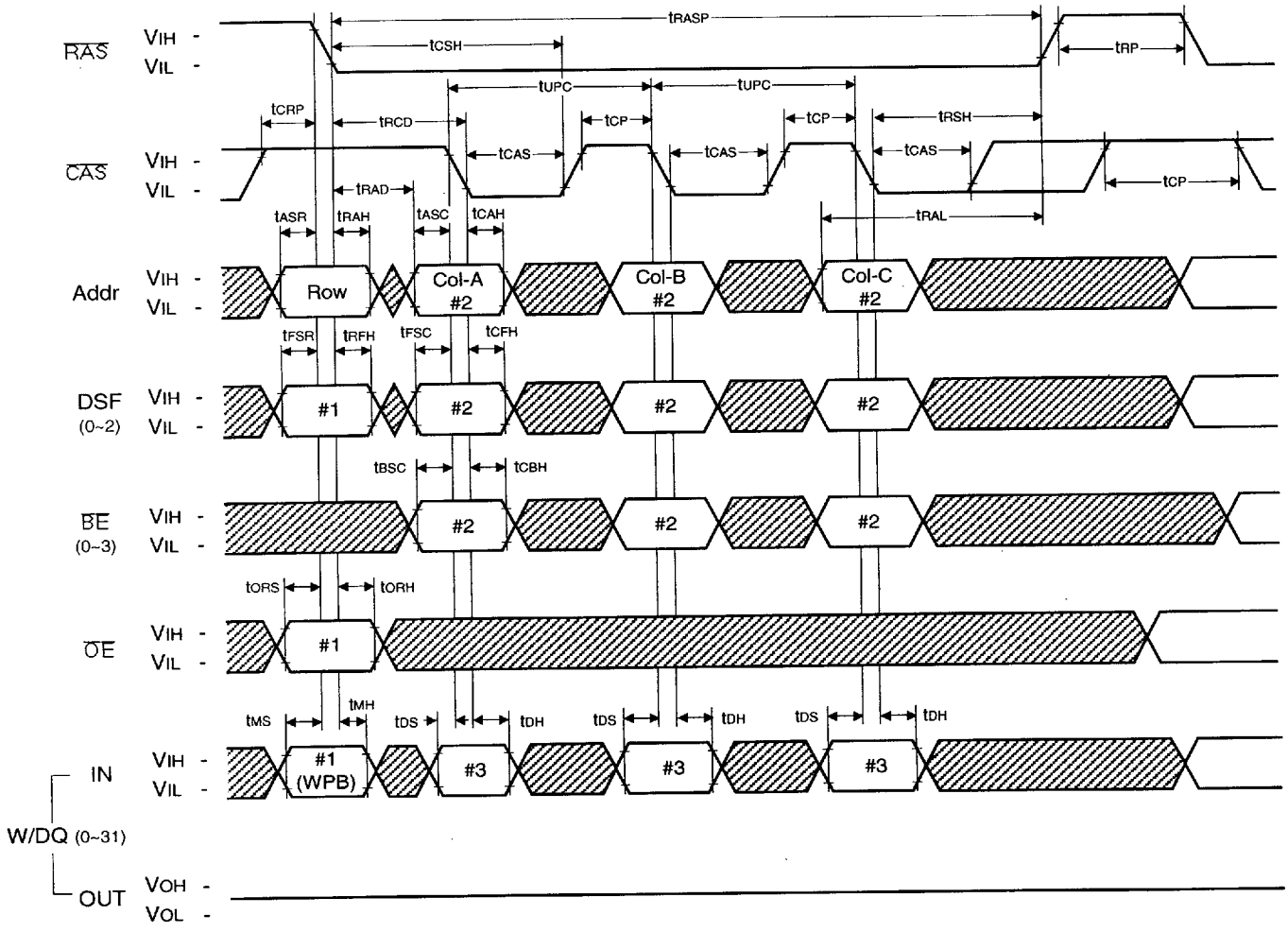


*Note ; #1,#2 : Refer to " Truth Tables"

: Don't Care

TIMING DIAGRAMS (continued)

ULTRA FAST PAGE BLOCK READ/WRITE(Latch)/WRITE(Color Register) AND SPLIT READ TRANSFER AND SPLIT READ TRANSFER WITH RESET CYCLES (Internal Operation)

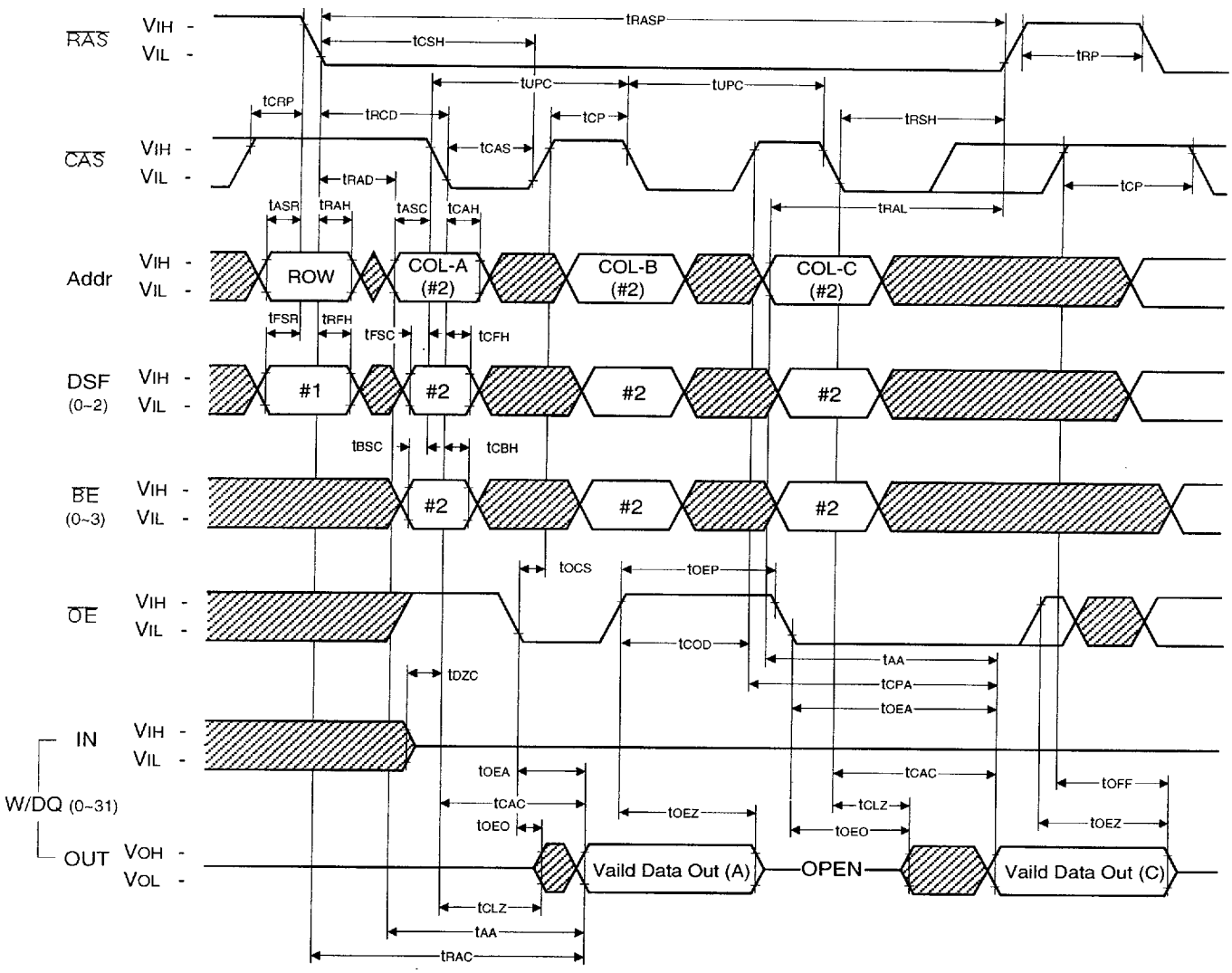


*Note ; #1,#2 : Refer to " Truth Tables"

: Don't Care

TIMING DIAGRAMS (continued)

ULTRA FAST PAGE READ (EDO) WITH $\overline{OE}$ CONTROLLED (DRAM, Color/Mask Register) CYCLE

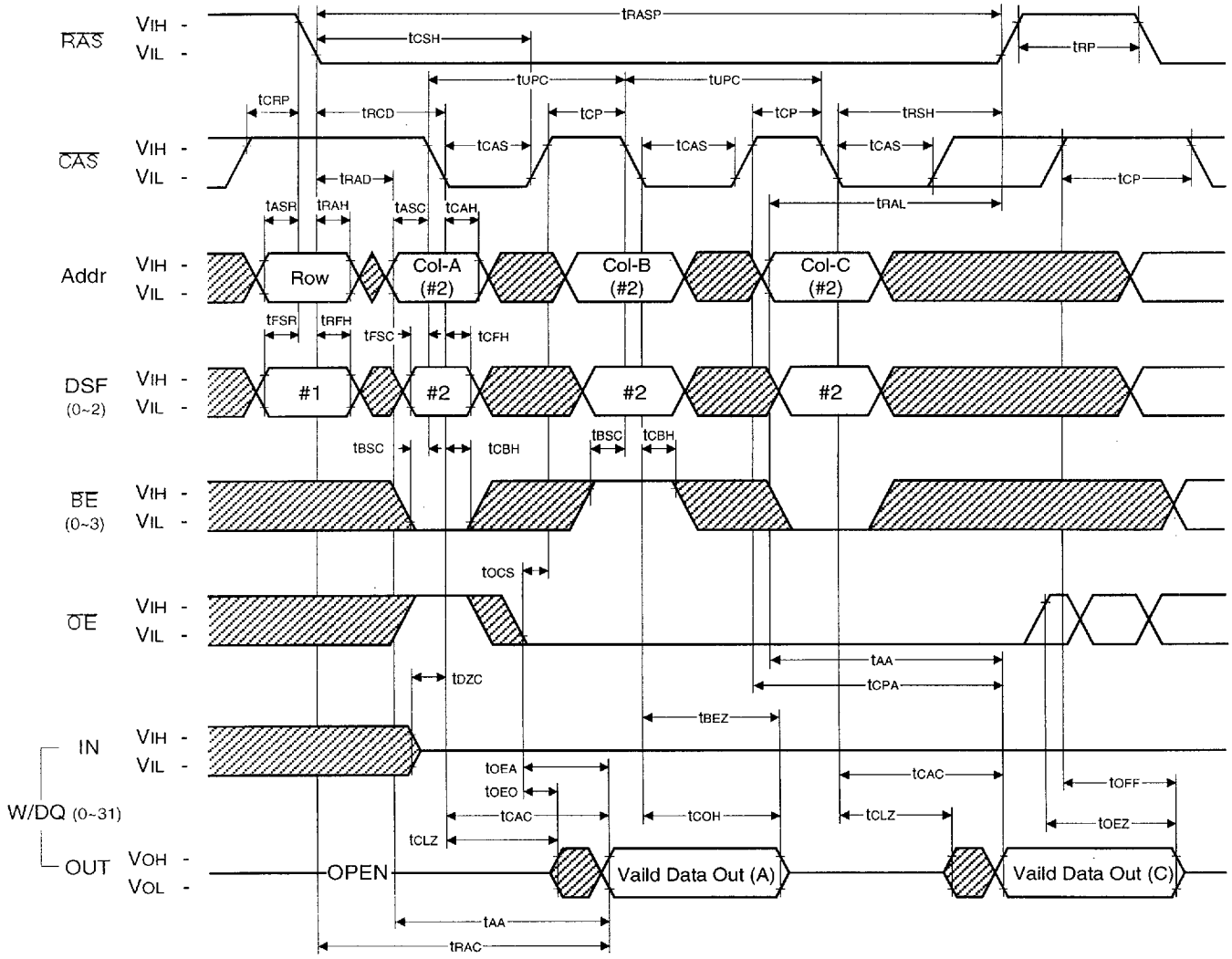


*Note ; #1,#2 : Refer to " Truth Tables"

: Don't Care

TIMING DIAGRAMS (continued)

ULTRA FAST PAGE READ (EDO) WITH $\overline{BE}$ CONTROLLED (DRAM, Color/Mask Register) CYCLE

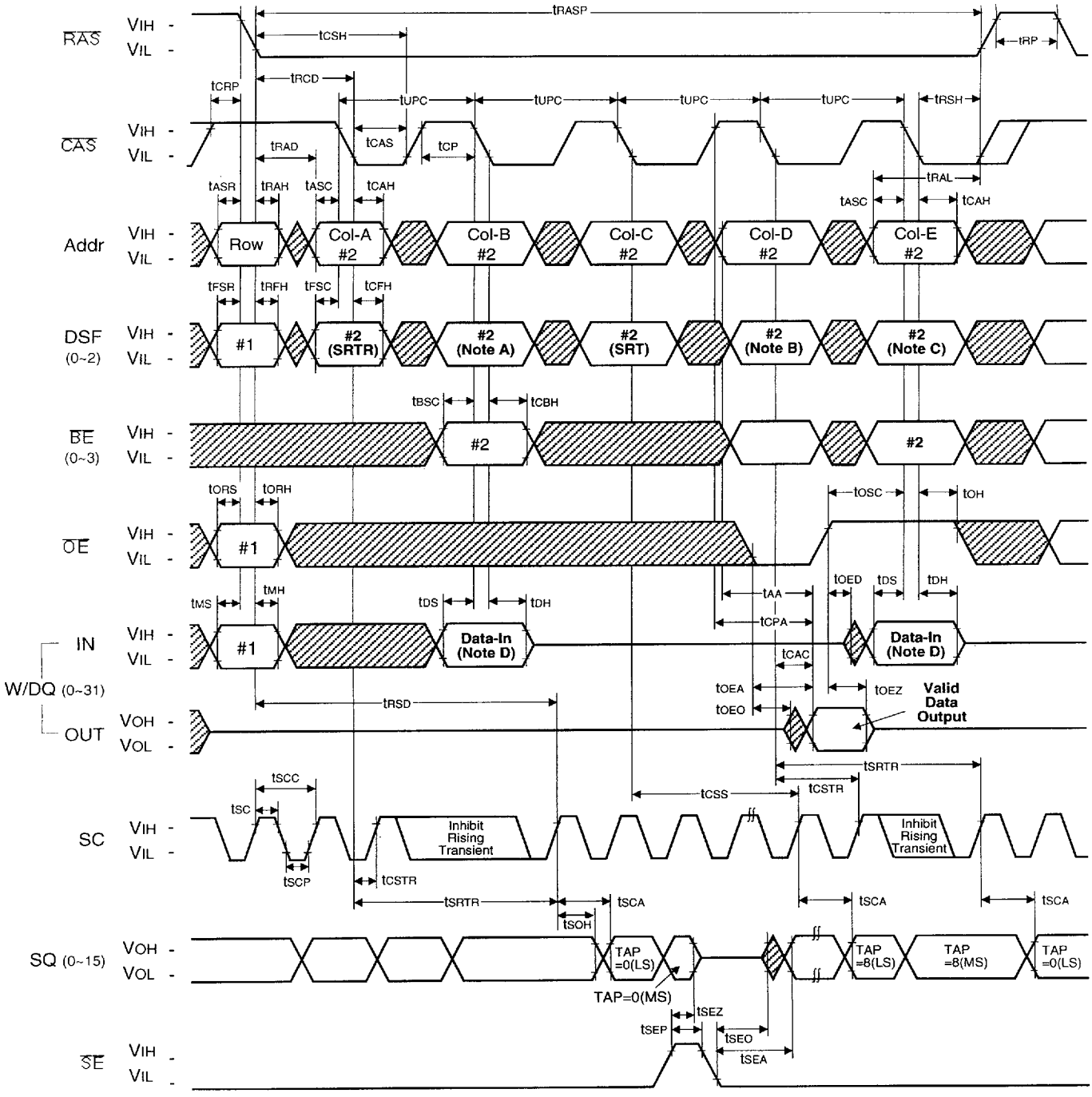


*Note ; #1,#2 : Refer to " Truth Tables"

: Don't Care

TIMING DIAGRAMS (continued)

SERIAL READ AND SPLIT READ TRANSFER CYCLE
(Mixes with Ultra Fast Page Internal Operations and Read/Write Cycle)



NOTE A: UFBR, UFBWL, UFBW8, SRT, LCR, LMR, UFW.

: Don't Care

NOTE B: READ CYCLES → UFR.

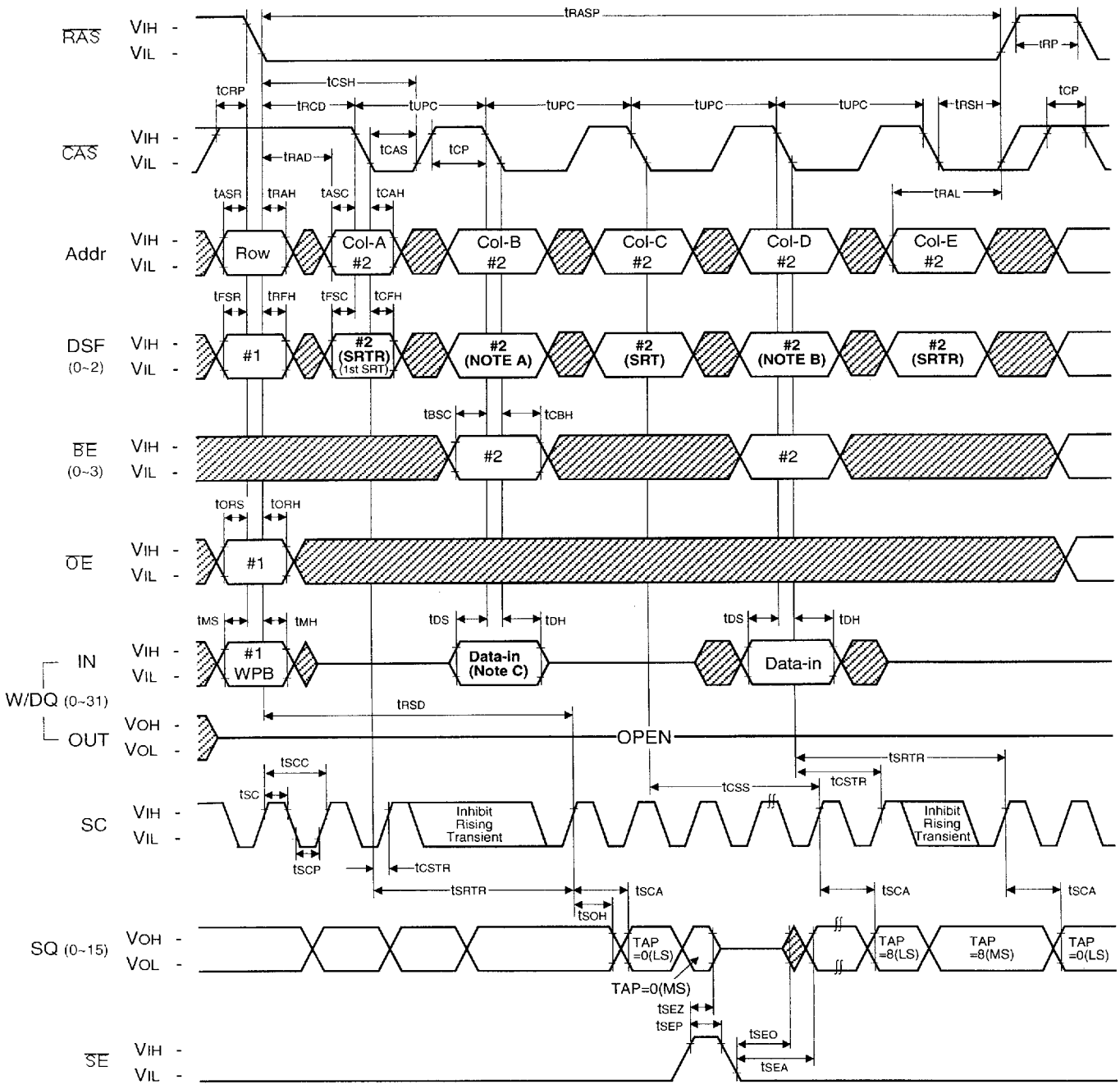
NOTE C: INTERNAL OPERATION CYCLES → UFBWL, UFBW8, SRT, SRTR.

NOTE D: DATA-IN IS NORMAL DATA FOR LCR, LMR and UFW CYCLES, BYTE MASKING DATA FOR UFBWL, UFBW8.

*Note ; #1,#2 : Refer to " Truth Tables"

TIMING DIAGRAMS (continued)

SERIAL READ AND SPLIT READ TRANSFER CYCLE WITH RESET CYCLE
(Mixes with Ultra Fast Page Internal Operations and Write/Load Cycle)



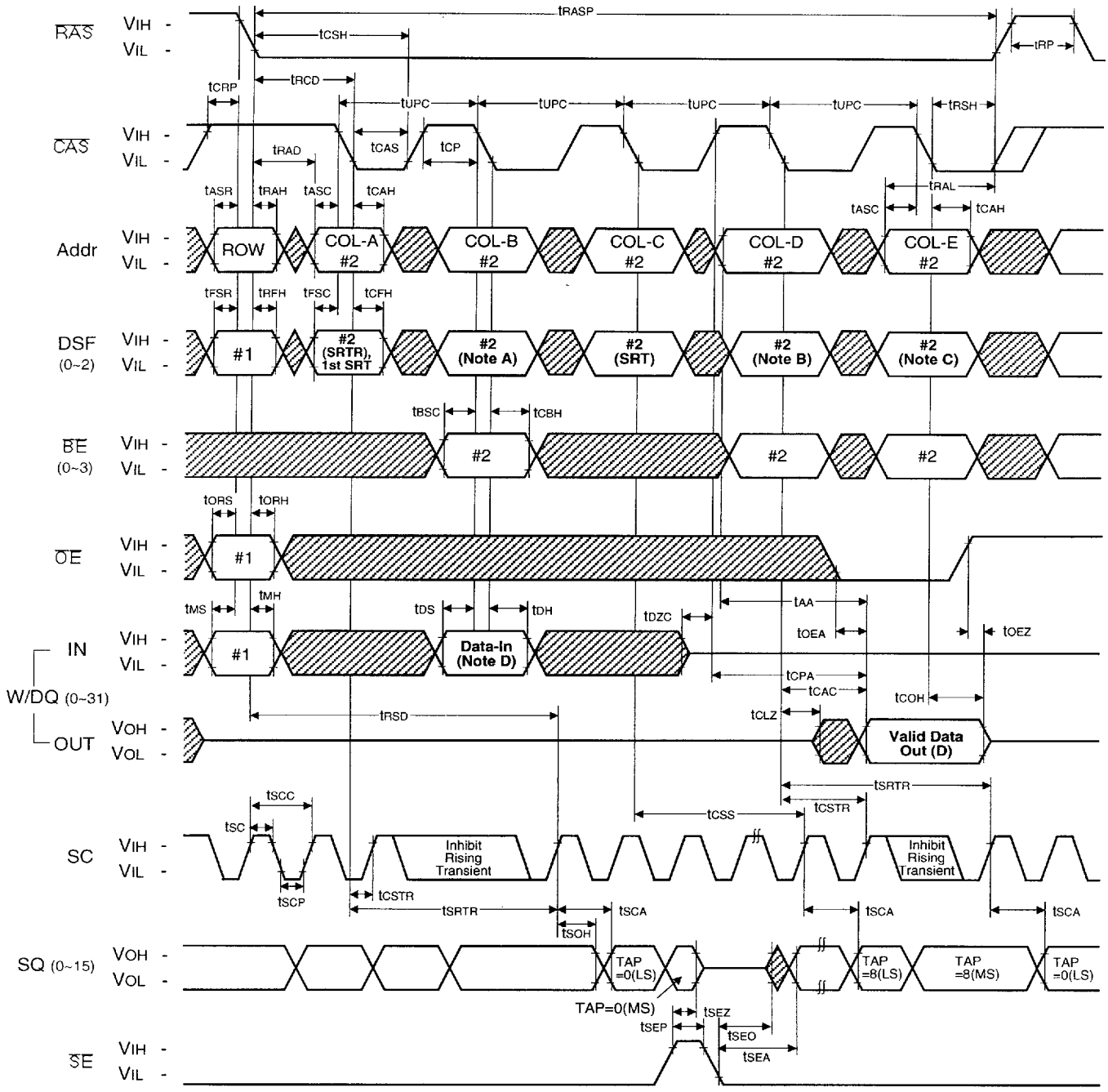
: Don't Care

NOTE A: INTERNAL OPERATION CYCLES → UFBR, SRT, UFBWL, UFBW8..
NOTE B: WRITE/LOAD CYCLES → LCR, LMR, UFW.
NOTE C: DATA-IN IS NORMAL DATA FOR LCR, LMR / BYTE MASKING DATA FOR UFBWL, UFBW8.

*Note ; #1,#2 : Refer to " Truth Tables"

TIMING DIAGRAMS (continued)

SERIAL READ, AND THE FIRST SRT, SRTR CYCLE AFTER POWER UP (Mixes with Ultra Fast Page Internal Operations and Read Cycle)



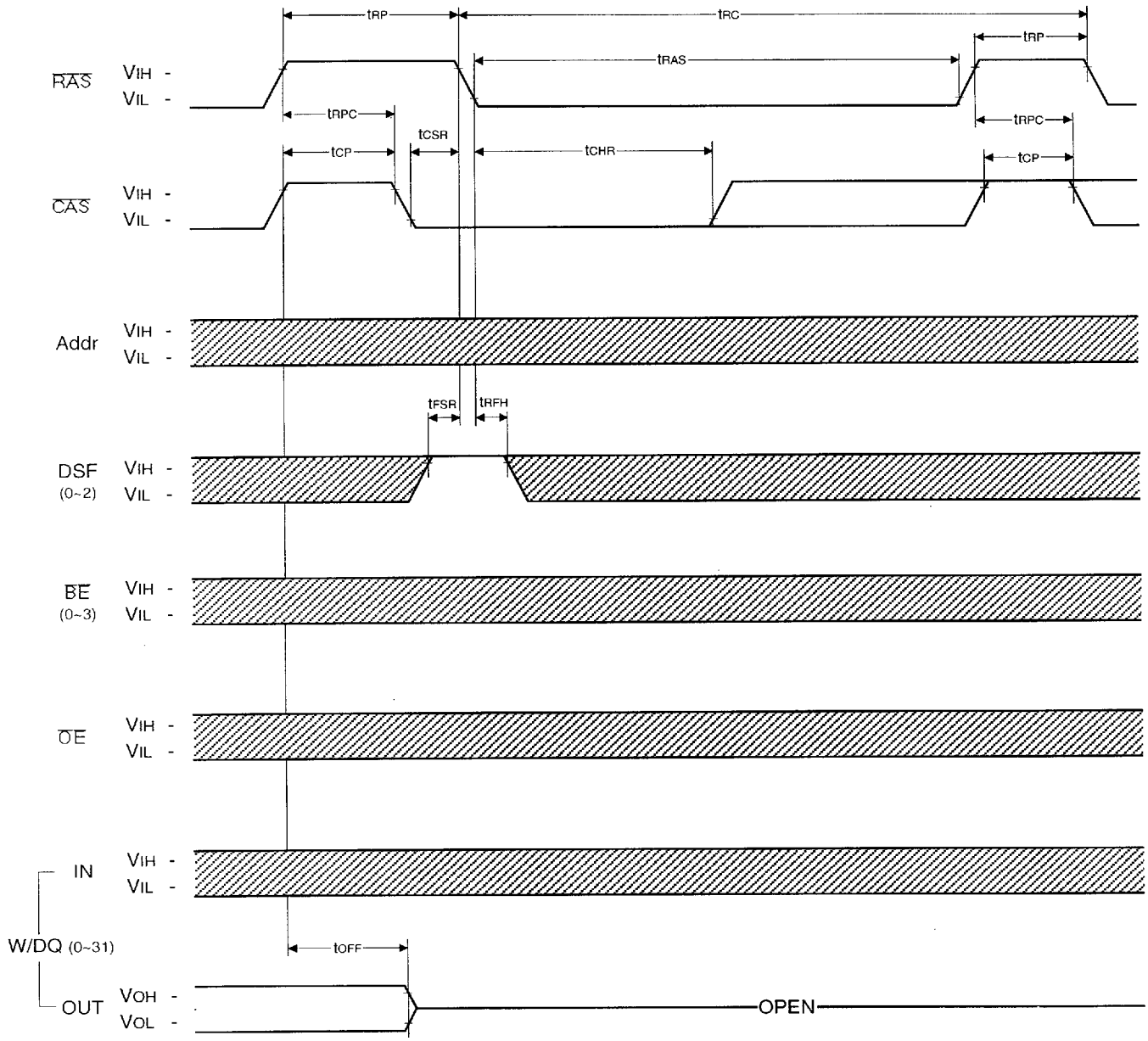
: Don't Care

NOTE A: UFBR, UFBWL, UFBW8, SRT, LCR, LMR, UFW.
NOTE B: READ CYCLES → UFR.
NOTE C: INTERNATION OPERATION CYCLES → UFBR, SRT, SRTR.
NOTE D: DATA-IN IS ONLY DATA FOR LCR, LMR and UFW CYCLES, BYTE MASKING DATA FOR UFBWL, UFBW8.

*Note ; #1,#2 : Refer to " Truth Tables"

TIMING DIAGRAMS (continued)

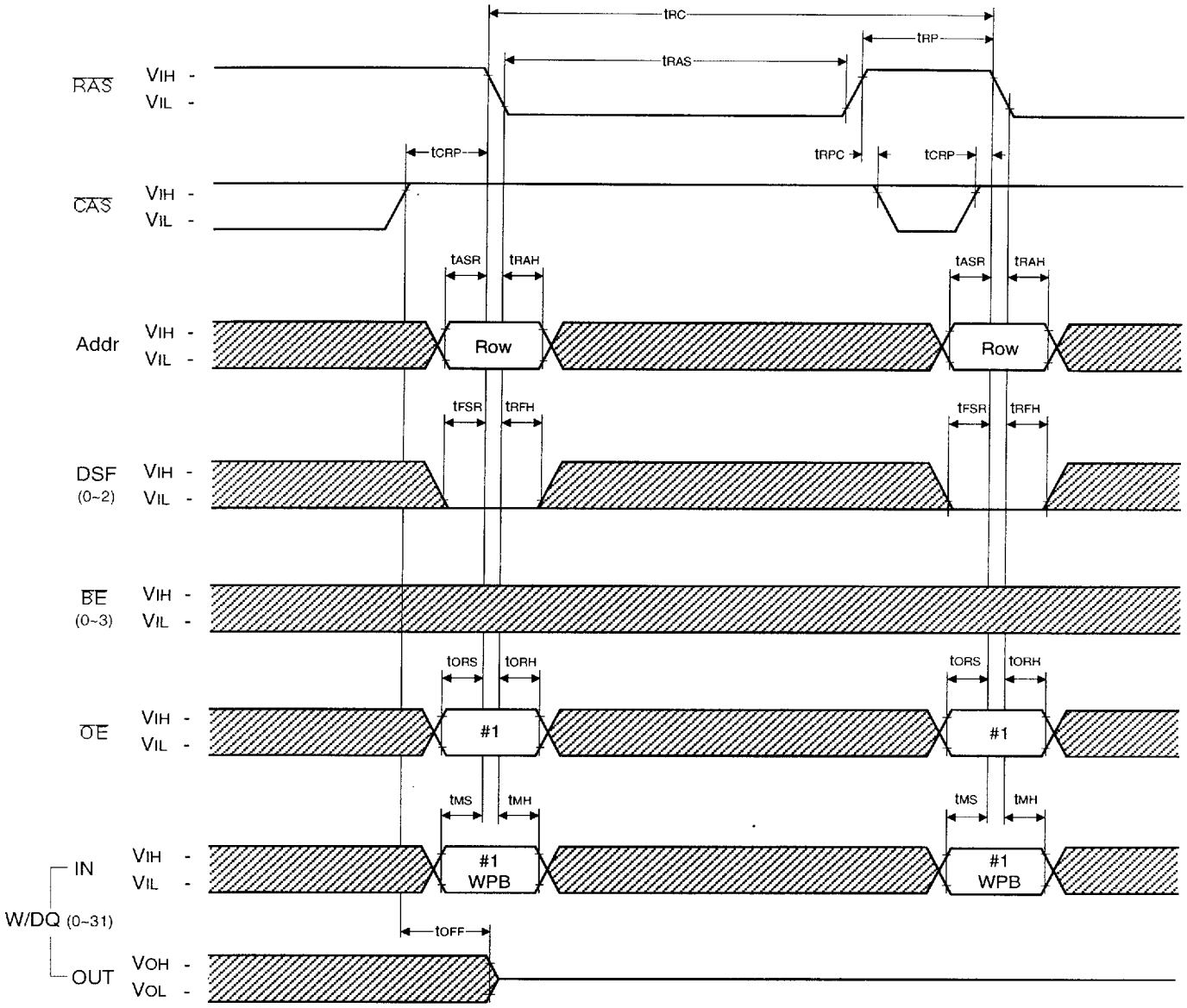
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



: Don't Care

TIMING DIAGRAMS (continued)

RAS ONLY REFRESH CYCLE



*Note ; #1,#2 : Refer to " Truth Tables"

: Don't Care

PACKAGE DIMENSION

Dimensions in Milimeters